# 3.3V CMOS 12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS AND BUS-HOLD

**IDT74ALVCHR162269A**

## FEATURES:

- **0.5 MICRON CMOS Technology**
- **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
- **ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)**
- **Vcc = 3.3V ± 0.3V, Normal Range**
- **Vcc = 2.7V to 3.6V, Extended Range**
- **Vcc = 2.5V ± 0.2V**
- **CMOS power levels (0.4µ W typ. static)**
- **Rail-to-Rail output swing for increased noise margin**
- **Available in SSOP and TSSOP packages**

## DRIVE FEATURES:

- **Balanced Output Drivers: ±12mA**
- **Low Switching Noise**

## APPLICATIONS:

- **3.3V high speed systems**
- **3.3V and lower voltage computing systems**

## DESCRIPTION:

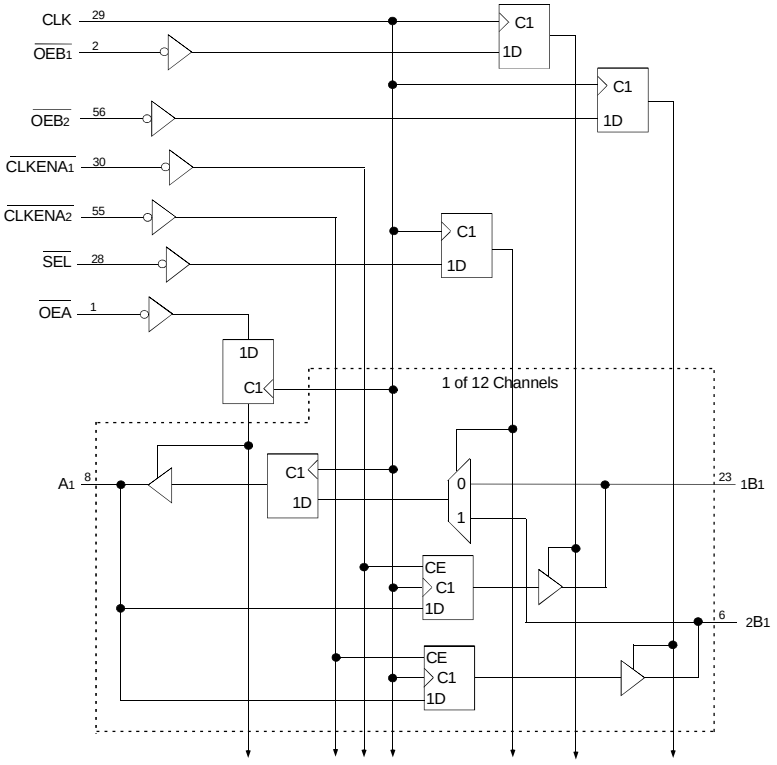
This 12-bit to 24-bit registered bus exchanger is used in applications in which two separate ports must be multiplexed onto, or demultiplexed from, a single port. It is particularly suitable as an interface between synchronous DRAMs and high-speed microprocessors.

Data is stored in the internal B-port registers on the low-to-high transition of the clock (CLK) input when the appropriate clock-enable ($\overline{CLKENA}$) inputs are low. Proper control of these inputs allows two sequential 12-bit words to be presented as a 24-bit word on the B-port. For data transfer in the B-to-A direction, a single storage register is provided. The select $\overline{SEL}$ line selects 1B or 2B data for the A outputs. The register on the A output permits the fastest possible data transfer, thus extending the period during which the data is valid on the bus. The control terminals are registered so that all transactions are synchronous with CLK. Data flow is controlled by the active-low output enables ($\overline{OEA}$, $\overline{OEB1}$ and $\overline{OEB2}$).

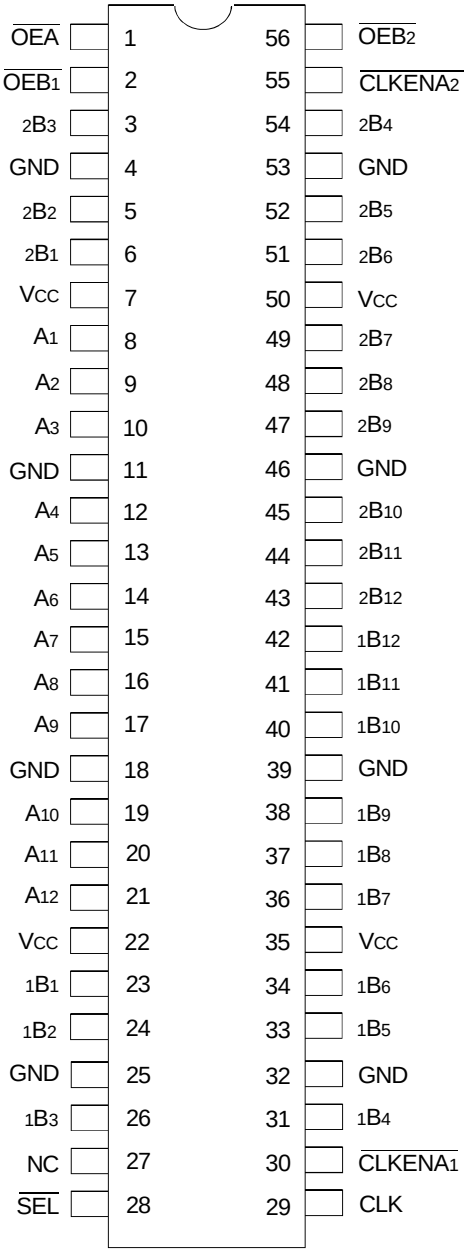
The ALVCHR162269A has series resistors in the device output structure which will significantly reduce line noise when used with light loads. This driver has been designed to drive ±12mA at the designated threshold levels.

The ALVCHR162269A has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

## FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION




**SSOP/ TSSOP**
**TOP VIEW**

## CAPACITANCE ($T_A$ = +25°C, F = 1.0MHz)

| Symbol | Parameter[1] | Conditions | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | 5 | 7 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0V | 7 | 9 | pF |
| $C_{I/O}$ | I/O Port Capacitance | $V_{IN}$ = 0V | 7 | 9 | pF |

**NOTE:**
1. As applicable to the device type.

## ABSOLUTE MAXIMUM RATINGS[1]

| Symbol | Description | Max | Unit |
|---|---|---|---|
| $V_{TERM}$[2] | Terminal Voltage with Respect to GND | –0.5 to +4.6 | V |
| $V_{TERM}$[3] | Terminal Voltage with Respect to GND | –0.5 to $V_{CC}$+0.5 | V |
| $T_{STG}$ | Storage Temperature | –65 to +150 | °C |
| $I_{OUT}$ | DC Output Current | –50 to +50 | mA |
| $I_{IK}$ | Continuous Clamp Current, $V_I$ < 0 or $V_I$ > $V_{CC}$ | ±50 | mA |
| $I_{OK}$ | Continuous Clamp Current, $V_O$ < 0 | –50 | mA |
| $I_{CC}$ $I_{SS}$ | Continuous Current through each $V_{CC}$ or GND | ±100 | mA |

**NOTES:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. $V_{CC}$ terminals.
3. All terminals except $V_{CC}$.

## FUNCTION TABLES[1]

**OUTPUT ENABLE**

| Inputs | | | Outputs | |
|---|---|---|---|---|
| CLK | $\overline{OEA}$ | $\overline{OEBx}$ | Ax | 1Bx, 2Bx |
| ↑ | H | H | Z | Z |
| ↑ | H | L | Z | Active |
| ↑ | L | H | Active | Z |
| ↑ | L | L | Active | Active |

**A-TO-B STORAGE ($\overline{OEB}$ = L)**

| Inputs | | | | Outputs | |
|---|---|---|---|---|---|
| $\overline{CLKENA1}$ | $\overline{CLKENA2}$ | CLK | Ax | 1Bx | 2Bx |
| H | H | X | X | 1B[2] | 2B[2] |
| L | X | ↑ | L | L | X |
| L | X | ↑ | H | H | X |
| X | L | ↑ | L | X | L |
| X | L | ↑ | H | X | H |

**B-TO-A STORAGE ($\overline{OEA}$ = L)**

| Inputs | | | | Outputs |
|---|---|---|---|---|
| CLK | $\overline{SEL}$ | 1Bx | 2Bx | Ax |
| X | H | X | X | A[2] |
| X | L | X | X | A[2] |
| ↑ | H | L | X | L |
| ↑ | H | H | X | H |
| ↑ | L | X | L | L |
| ↑ | L | X | H | H |

**NOTES:**
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance
   ↑ = LOW-to-HIGH transition
2. Output level before the indicated steady-state input conditions were established.

## PIN DESCRIPTION

| Pin Names | I/O | Description |
|---|---|---|
| $A_{X(1:12)}$ | I/O | Bidirectional Data Port A. Usually connected to the CPU's Address/Data bus.[1] |
| $1B_{X(1:12)}$ | I/O | Bidirectional Data Port 1B. Usually connected to the even path or even bank of memory.[1] |
| $2B_{X(1:12)}$ | I/O | Bidirectional Data Port 2B. Usually connected to the odd path or odd bank of memory.[1] |
| CLK | I | Clock Input |
| $\overline{CLKENA1}$ | I | Clock Enable Input for the A-1B Register. If $\overline{CLKENA1}$ is LOW during the rising edge of CLK, data will be clocked into register A-1B (Active LOW). |
| $\overline{CLKENA2}$ | I | Clock Enable Input for the A-2B Register. If $\overline{CLKENA2}$ is LOW during the rising edge of CLK, data will be clocked into register A-2B (Active LOW). |
| $\overline{SEL}$ | I | 1B or 2B Port Selection. When HIGH during the rising edge of CLK, $\overline{SEL}$ enables data transfer from 1B Port to A Port. When LOW during the rising edge of CLK, $\overline{SEL}$ enables data transfer from 2B Port to A Port. |
| $\overline{OEA}$ | I | Synchronous Output Enable for A Port (Active LOW) |
| $\overline{OEB1}$ | I | Synchronous Output Enable for 1B Port (Active LOW) |
| $\overline{OEB2}$ | I | Synchronous Output Enable for 2B Port (Active LOW) |

**NOTE:**
1. These pins have "Bus-Hold". All other pins are standard inputs, outputs, or I/Os.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: $T_A$ = –40°C to +85°C

| Symbol | Parameter | Test Conditions | | Min. | Typ.[1] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage Level | $V_{CC}$ = 2.3V to 2.7V | | 1.7 | — | — | V |
| | | $V_{CC}$ = 2.7V to 3.6V | | 2 | — | — | |
| $V_{IL}$ | Input LOW Voltage Level | $V_{CC}$ = 2.3V to 2.7V | | — | — | 0.7 | V |
| | | $V_{CC}$ = 2.7V to 3.6V | | — | — | 0.8 | |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = 3.6V | $V_I$ = $V_{CC}$ | — | — | ±5 | µA |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = 3.6V | $V_I$ = GND | — | — | ±5 | µA |
| $I_{OZH}$ | High Impedance Output Current | $V_{CC}$ = 3.6V | $V_O$ = $V_{CC}$ | — | — | ±10 | µA |
| $I_{OZL}$ | (3-State Output pins) | | $V_O$ = GND | — | — | ±10 | |
| $V_{IK}$ | Clamp Diode Voltage | $V_{CC}$ = 2.3V, $I_{IN}$ = –18mA | | — | –0.7 | –1.2 | V |
| $V_H$ | Input Hysteresis | $V_{CC}$ = 3.3V | | — | 100 | — | mV |
| $I_{CCL}$<br>$I_{CCH}$<br>$I_{CCZ}$ | Quiescent Power Supply Current | $V_{CC}$ = 3.6V<br>$V_{IN}$ = GND or $V_{CC}$ | | — | 0.1 | 40 | µA |
| $\Delta I_{CC}$ | Quiescent Power Supply Current Variation | One input at $V_{CC}$ - 0.6V, other inputs at $V_{CC}$ or GND | | — | — | 750 | µA |

**NOTE:**
1. Typical values are at $V_{CC}$ = 3.3V, +25°C ambient.

## BUS-HOLD CHARACTERISTICS

| Symbol | Parameter[1] | Test Conditions | | Min. | Typ.[2] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $I_{BHH}$ | Bus-Hold Input Sustain Current | $V_{CC}$ = 3V | $V_I$ = 2V | –75 | — | — | µA |
| $I_{BHL}$ | | | $V_I$ = 0.8V | 75 | — | — | |
| $I_{BHH}$ | Bus-Hold Input Sustain Current | $V_{CC}$ = 2.3V | $V_I$ = 1.7V | –45 | — | — | µA |
| $I_{BHL}$ | | | $V_I$ = 0.7V | 45 | — | — | |
| $I_{BHHO}$ | Bus-Hold Input Overdrive Current | $V_{CC}$ = 3.6V | $V_I$ = 0 to 3.6V | — | — | ±500 | µA |
| $I_{BHLO}$ | | | | | | | |

**NOTES:**
1. Pins with Bus-Hold are identified in the pin description.
2. Typical values are at $V_{CC}$ = 3.3V, +25°C ambient.

## OUTPUT DRIVE CHARACTERISTICS

| Symbol | Parameter | Test Conditions[1] | | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = 2.3V to 3.6V | $I_{OH}$ = – 0.1mA | $V_{CC}$ – 0.2 | — | V |
| | | $V_{CC}$ = 2.3V | $I_{OH}$ = – 4mA | 1.9 | — | |
| | | | $I_{OH}$ = – 6mA | 1.7 | — | |
| | | $V_{CC}$ = 2.7V | $I_{OH}$ = – 4mA | 2.2 | — | |
| | | | $I_{OH}$ = – 8mA | 2 | — | |
| | | $V_{CC}$ = 3V | $I_{OH}$ = – 6mA | 2.4 | — | |
| | | | $I_{OH}$ = – 12mA | 2 | — | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = 2.3V to 3.6V | $I_{OL}$ = 0.1mA | — | 0.2 | V |
| | | $V_{CC}$ = 2.3V | $I_{OL}$ = 4mA | — | 0.4 | |
| | | | $I_{OL}$ = 6mA | — | 0.55 | |
| | | $V_{CC}$ = 2.7V | $I_{OL}$ = 4mA | — | 0.4 | |
| | | | $I_{OL}$ = 8mA | — | 0.6 | |
| | | $V_{CC}$ = 3V | $I_{OL}$ = 6mA | — | 0.55 | |
| | | | $I_{OL}$ = 12mA | — | 0.8 | |

**NOTE:**
1. $V_{IH}$ and $V_{IL}$ must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate $V_{CC}$ range. $T_A$ = – 40°C to + 85°C.

## OPERATING CHARACTERISTICS, $T_A$ = 25°C

| Symbol | Parameter | Test Conditions | $V_{CC}$ = 2.5V ± 0.2V Typical | $V_{CC}$ = 3.3V ± 0.3V Typical | Unit |
|---|---|---|---|---|---|
| $C_{PD}$ | Power Dissipation Capacitance Outputs enabled | $C_L$ = 0pF, f = 10Mhz | 142 | 172 | pF |
| $C_{PD}$ | Power Dissipation Capacitance Outputs disabled | | 115 | 129 | |

## SWITCHING CHARACTERISTICS(1)

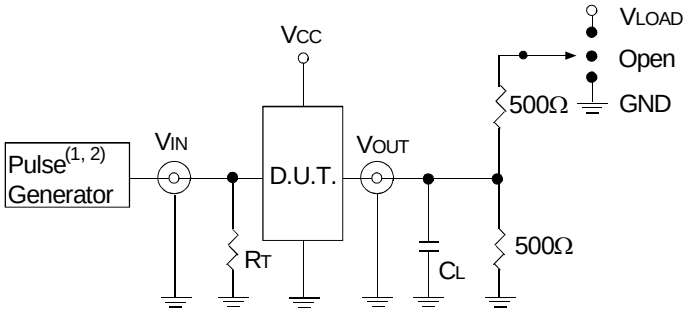
| Symbol | Parameter | $V_{CC}$ = 2.5V ± 0.2V | | $V_{CC}$ = 2.7V | | $V_{CC}$ = 3.3V ± 0.15V | | $V_{CC}$ = 3.3V ± 0.3V | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $f_{CLOCK}$ | Clock Frequency | — | 95 | — | 115 | — | 135 | — | 135 | MHz |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>CLK to xBx | 2.3 | 7.7 | — | 6.9 | 2.3 | 5 | 2.2 | 5.8 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>CLK to Ax | 1.9 | 6.4 | — | 5.8 | 2 | 4 | 2 | 5.2 | ns |
| $t_{PZH}$<br>$t_{PZL}$ | Output Enable Time<br>CLK to xBx | 2.5 | 7.7 | — | 6.9 | 2.3 | 5 | 2.3 | 5.8 | ns |
| $t_{PZH}$<br>$t_{PZL}$ | Output Enable Time<br>CLK to Ax | 2.2 | 6.7 | — | 6 | 2.1 | 4.3 | 2.1 | 5.3 | ns |
| $t_{PHZ}$<br>$t_{PLZ}$ | Output Disable Time<br>CLK to xBx | 3.3 | 8.1 | — | 6.7 | 2.3 | 5.3 | 2.4 | 6 | ns |
| $t_{PHZ}$<br>$t_{PLZ}$ | Output Disable Time<br>CLK to Ax | 2.7 | 8 | — | 6.2 | 2.2 | 5.4 | 2.1 | 6 | ns |
| $t_{SU}$ | Set-Up Time, Ax data before CLK↑ | 1.4 | — | 1.4 | — | 0.9 | — | 1 | — | ns |
| $t_{SU}$ | Set-Up Time, Bx data before CLK↑ | 1.6 | — | 1.5 | — | 1 | — | 1.1 | — | ns |
| $t_{SU}$ | Set-Up Time, $\overline{SEL}$ before CLK↑ | 0.8 | — | 1.1 | — | 1.3 | — | 1.3 | — | ns |
| $t_{SU}$ | Set-Up Time, $\overline{CLKENA1}$ or $\overline{CLKENA2}$ before CLK↑ | 0.8 | — | 1 | — | 0.7 | — | 0.8 | — | ns |
| $t_{SU}$ | Set-Up Time, $\overline{OEBx}$ or $\overline{OEA}$ before CLK↑ | 1.7 | — | 1.6 | — | 1.1 | — | 1.2 | — | ns |
| $t_H$ | Hold Time, Ax data after CLK↑ | 0.9 | — | 0.9 | — | 1.1 | — | 1.2 | — | ns |
| $t_H$ | Hold Time, Bx data after CLK↑ | 0.8 | — | 0.6 | — | 0.8 | — | 1 | — | ns |
| $t_H$ | Hold Time, $\overline{SEL}$ after CLK↑ | 1.1 | — | 0.8 | — | 1.6 | — | 1.7 | — | ns |
| $t_H$ | Hold Time, $\overline{CLKENA1}$ or $\overline{CLKENA2}$ after CLK↑ | 1.4 | — | 1 | — | 1.4 | — | 1.6 | — | ns |
| $t_H$ | Hold Time, $\overline{OEBx}$ or $\overline{OEA}$ after CLK↑ | 0.9 | — | 0.8 | — | 1 | — | 1.2 | — | ns |
| $t_W$ | Pulse Width, CLK HIGH or LOW | 5.2 | — | 4.3 | — | 3.3 | — | 3.3 | — | ns |
| $t_{SK}(o)$ | Output Skew(2) | — | — | — | — | — | 500 | — | 500 | ps |

**NOTES:**
1. See TEST CIRCUITS AND WAVEFORMS. $T_A$ = – 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

# TEST CIRCUITS AND WAVEFORMS

## TEST CONDITIONS

| Symbol | $V_{CC}^{(1)}$=3.3V±0.3V | $V_{CC}^{(1)}$=2.7V | $V_{CC}^{(2)}$=2.5V±0.2V | Unit |
|---|---|---|---|---|
| $V_{LOAD}$ | 6 | 6 | 2 x Vcc | V |
| $V_{IH}$ | 2.7 | 2.7 | Vcc | V |
| $V_T$ | 1.5 | 1.5 | Vcc / 2 | V |
| $V_{LZ}$ | 300 | 300 | 150 | mV |
| $V_{HZ}$ | 300 | 300 | 150 | mV |
| $C_L$ | 50 | 50 | 30 | pF |




***Test Circuit for All Outputs***

**DEFINITIONS:**

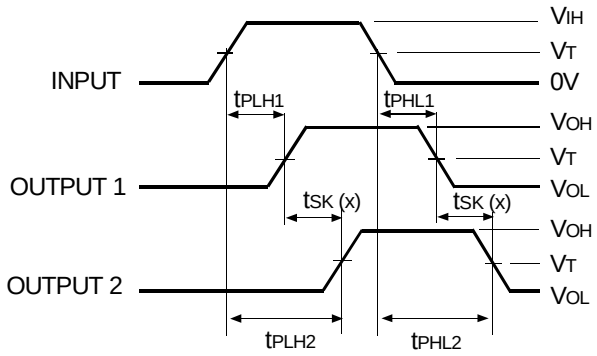
$C_L$ = Load capacitance: includes jig and probe capacitance.
$R_T$ = Termination resistance: should be equal to $Z_{OUT}$ of the Pulse Generator.

**NOTES:**

1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $t_F$ ≤ 2.5ns; $t_R$ ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $t_F$ ≤ 2ns; $t_R$ ≤ 2ns.

## SWITCH POSITION

| Test | Switch |
|---|---|
| Open Drain<br>Disable Low<br>Enable Low | $V_{LOAD}$ |
| Disable High<br>Enable High | GND |
| All Other Tests | Open |

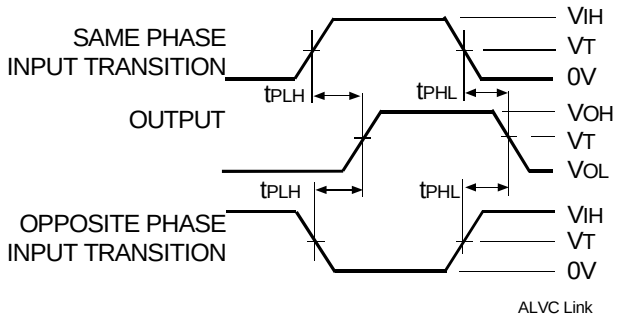



$t_{SK(x)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

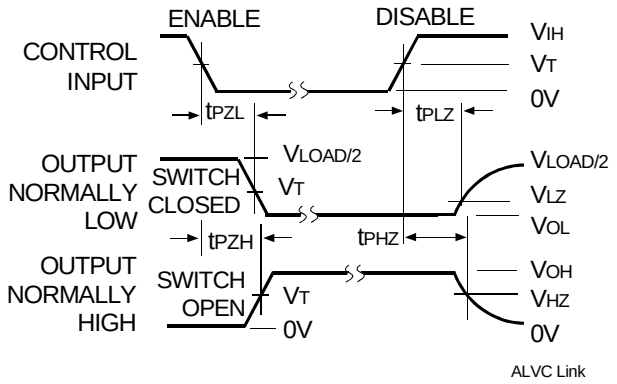
***Output Skew - $t_{SK(x)}$***

**NOTES:**

1. For $t_{SK}$(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For $t_{SK}$(b) OUTPUT1 and OUTPUT2 are in the same bank.



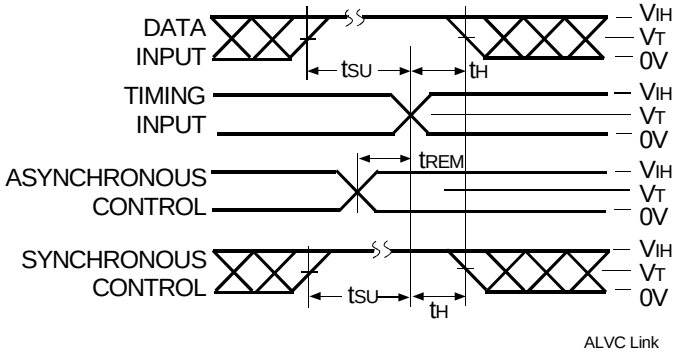

***Propagation Delay***



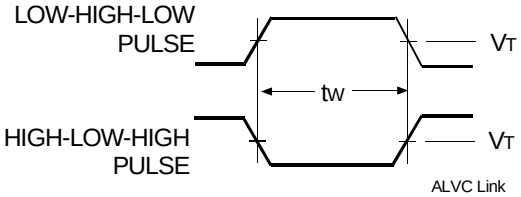

***Enable and Disable Times***

**NOTE:**

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

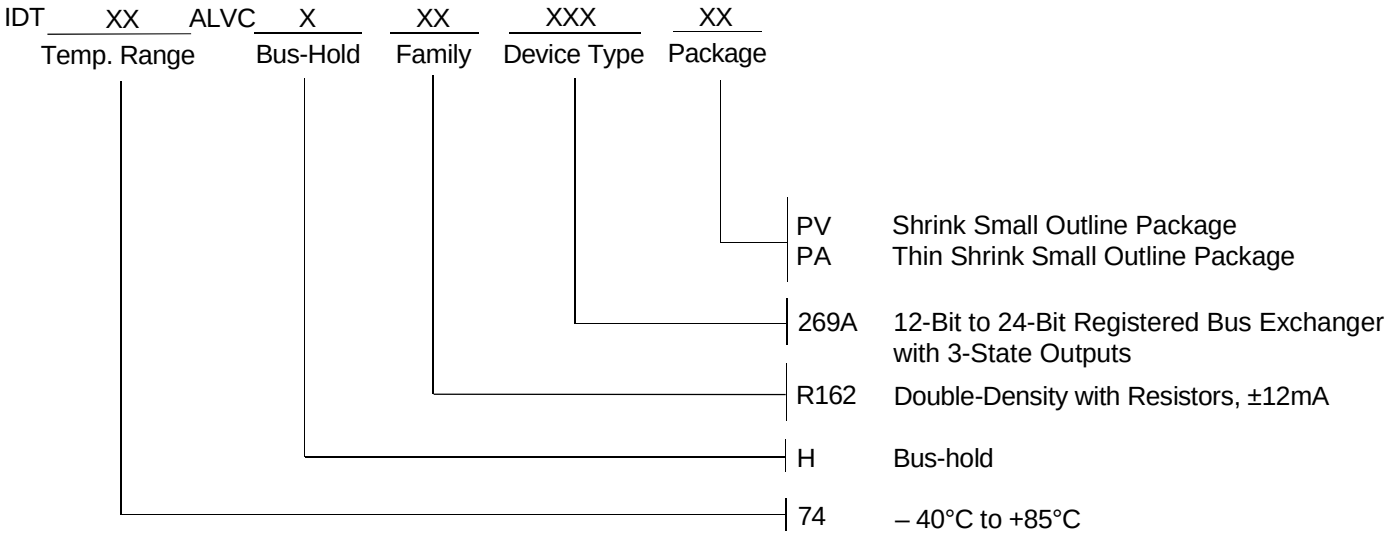



***Set-up, Hold, and Release Times***




***Pulse Width***

## ORDERING INFORMATION

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