STANDARD MICROSYSTEMS CORPORATION

SIO10N268

Advanced Notebook I/O for ISA or LPC Designs with X-Bus Interface for I/O, Memory, and FWH Emulation and Four Serial Ports

Datasheet

Product Features

- 3.3 Volt Operation (5 Volt Tolerant)
- PC99, PC01, ACPI 1.0 Compliant
- LPC or ISA Interface
  - SIO10N268 offers two modes of operation: LPC Mode or ISA Mode. These modes are jumper selectable.
- X-Bus Interface (LPC Mode Only)
  - Three chip selects (2 I/O and 1 Memory)
  - 8-bit data transfers
  - Support for up to 2MB Flash
  - Interfaces with 3V memory devices
  - Support for up to two external I/O components
  - Offers three modes of operation for I/O devices
  - Provides FWH Emulation
- Serial IRQ Compatible with Serialized IRQ Support for PCI Systems
- Programmable Wake-up Event (PME) Interface
- (33) General Purpose Input/Output Pins
- System Management Interrupt
- 2.88MB Super I/O Floppy Disk Controller
  - Licensed CMOS 765B Floppy Disk Controller
  - Software and Register Compatible with SMSC's Proprietary 82077AA Compatible Core
  - Supports Two Floppy Drives Directly
  - Configurable Open Drain/Push-Pull Output Drivers
  - Supports Vertical Recording Format
  - 16-Byte Data FIFO
  - 100% IBM Compatibility
  - Detects All Overrun and Underrun Conditions
  - Sophisticated Power Control Circuitry (PCC) Including Multiple Power Down Modes for Reduced Power Consumption
  - DMA Enable Logic
  - Data Rate and Drive Control Registers
  - 480 Address, Up to 15 IRQ and Four DMA Options
- Floppy Disk Available on Parallel Port Pins (ACPI Compliant)
  - Enhanced Digital Data Separator
  - 2 Mbps, 1 Mbps, 500 Kbps, 300 Kbps, 250 Kbps Data Rates
  - Programmable Precompensation Modes
- Serial Ports
  - Four Full Function Serial Ports
  - High Speed NS16C550 Compatible UARTs with Send/Receive 16-Byte FIFOs
  - Supports 230k and 460k Baud
  - Programmable Baud Rate Generator
  - Modem Control Circuitry
  - 480 Address and 15 IRQ Options
- Infrared Communications Controller
  - IrDA v1.2 (4Mbps), HPSIR, ASKIR, Consumer IR Support
  - 2 IR Ports
  - 96 Base I/O Address, 15 IRQ, and 4 DMA Options
- Multi-Mode Parallel Port with ChiProtect
  - Standard Mode IBM PC/XT, PC/AT, and PS/2 Compatible Bi-directional Parallel Port
  - Enhanced Parallel Port (EPP) Compatible - EPP 1.7 and EPP 1.9 (IEEE 1284 Compliant)
  - IEEE 1284 Compliant Enhanced Capabilities Port (ECP)
  - ChiProtect Circuitry for Protection
  - 480 Address, Up to 15 IRQ, and Four DMA Options
- Two LED Drivers with blinking options
- Watch Dog Timer with optional output pin
- 128 Pin TQFP Package

PRELIMINARY

ORDERING INFORMATION

Order Number(s):

SIO10N268-NE for 128 Pin TQFP Package

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Chapter 1 General Description

The SIO10N268 is a single chip I/O device that can be used on the ISA or LPC bus. Bus selection is accomplished as a jumper option. Offering the same part with two system busses enables easy migration from an ISA architecture to the LPC generation enabling the preservation of design techniques and BIOS.

The SIO10N268 is a 3.3V operational (5.0V tolerant), PC 99/2001, and ACPI 1.0 compliant Super I/O Controller. This device includes SMSC's true CMOS 765B floppy disk controller with advanced digital data separator and SMSC's Multi-Mode parallel port with ChiProtect circuitry plus EPP and ECP support.

Each variation of the part also includes 33 GPIO pins, support for two LED's with blinking option, and a WatchDog Timer (WDT) with optional output pin. The SIO10N268 includes (4) 16C550 compatible UARTs. One UART includes additional support for a Serial Infrared Interface that complies with IrDA v1.2 (Fast IR), HPSIR, and ASKIR formats, as well as Consumer IR.

SIO10N268, when LPC Mode is selected, implements the LPC bus interface. In this mode, the X-Bus Interface is enabled to interface to external I/O devices that have an 8-bit data bus and to standard ISA memory devices, up to 2MB, which can serve as BIOS flash.

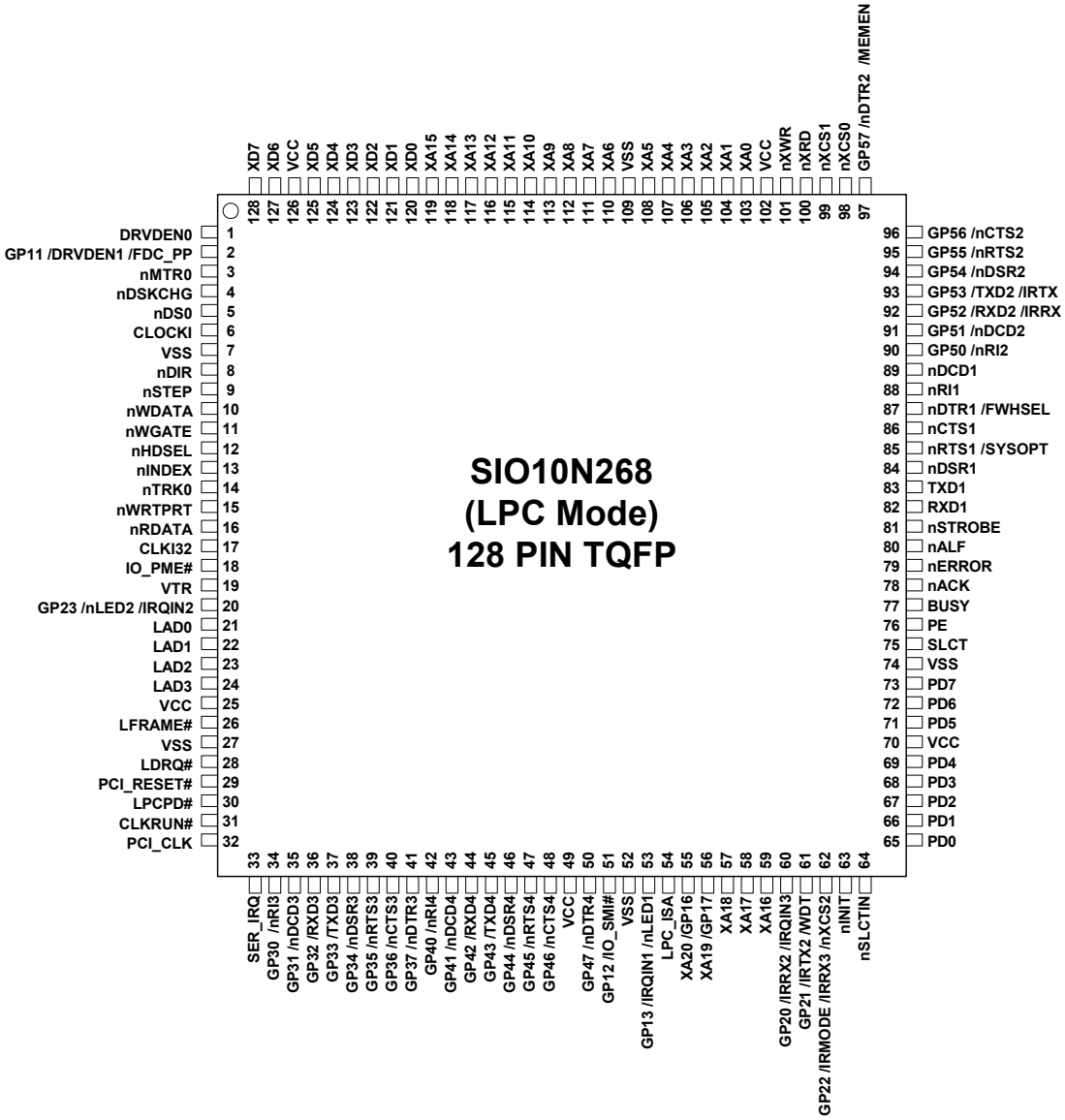
SIO10N268, when ISA Mode is selected, supports the ISA Plug-and-Play Standard (Version 1.0a). The I/O Address, DMA Channel and Hardware IRQ of each device in the part may be reprogrammed through the internal configuration registers.

Chapter 2 Pin Layouts

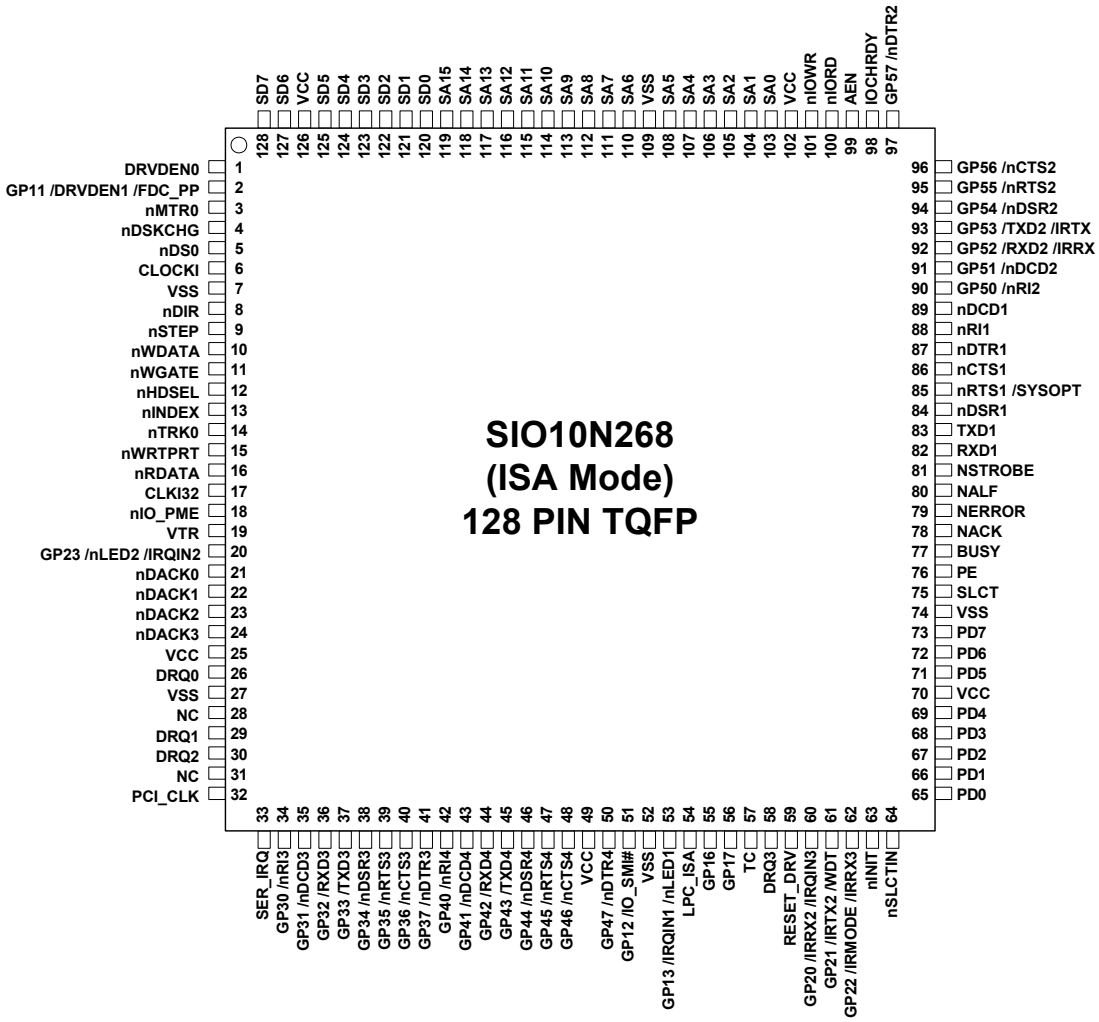
The SIO10N268 may be implemented in LPC Mode or ISA Mode. The following sections show the pin layouts for each of these modes.

NOTE: The mode of operation is selected by the LPC_ISA pin. The LPC_ISA pin should be connected directly to VCC to select ISA mode - a pull-up resistor may be used if it is of a low value e.g., 1kohm. It can either be left unconnected or connected to ground to select LPC mode. The pin has a 30uA internal pulldown.

2.1 LPC Mode



2.2 ISA Mode



Chapter 3 Pin Configurations for SIO10N268

The following tables show the pinout for the SIO10N268 in LPC Mode and ISA Mode. The mode of operation is selected by the LPC_ISA pin. The LPC_ISA pin should be connected directly to VCC to select ISA mode - a pull-up resistor may be used if it is of a low value e.g., 1kohm. It can either be left unconnected or connected to ground to select LPC mode. The pin has a 30uA internal pulldown.

Table 3.1 - SIO10N268 LPC Mode

PIN #	NAME	PIN #	NAME	PIN #	NAME	PIN #	NAME
1	DRVDEN0	33	SER_IRQ	65	PD0	97	GP57 /nDTR2 /MEMEN
2	GP11 /DRVDEN1 /FDC_PP	34	GP30 /nRI3	66	PD1	98	nXCS0
3	nMTR0	35	GP31 /nDCD3	67	PD2	99	nXCS1
4	nDSKCHG	36	GP32 /RXD3	68	PD3	100	nXRD
5	nDS0	37	GP33 /TXD3	69	PD4	101	nXWR
6	CLOCKI	38	GP34 /nDSR3	70	VCC	102	VCC
7	VSS	39	GP35 /nRTS3	71	PD5	103	XA0
8	nDIR	40	GP36 /nCTS3	72	PD6	104	XA1
9	nSTEP	41	GP37 /nDTR3	73	PD7	105	XA2
10	nWDATA	42	GP40 /nRI4	74	VSS	106	XA3
11	nWGATE	43	GP41 /nDCD4	75	SLCT	107	XA4
12	nHDSEL	44	GP42 /RXD4	76	PE	108	XA5
13	nINDEX	45	GP43 /TXD4	77	BUSY	109	VSS
14	nTRK0	46	GP44 /nDSR4	78	nACK	110	XA6
15	nWRTPRT	47	GP45 /nRTS4	79	nERROR	111	XA7
16	nRDATA	48	GP46 /nCTS4	80	nALF	112	XA8
17	CLKI32	49	VCC	81	nSTROBE	113	XA9
18	IO_PME#	50	GP47 /nDTR4	82	RXD1	114	XA10
19	VTR	51	GP12 /IO_SMI#	83	TXD1	115	XA11
20	GP23 /nLED2 /IRQIN2	52	VSS	84	nDSR1	116	XA12
21	LAD0	53	GP13 /IRQIN1 /nLED1	85	nRTS1 /SYSOPT	117	XA13
22	LAD1	54	LPC_ISA	86	nCTS1	118	XA14
23	LAD2	55	XA20 /GP16	87	nDTR1 /FWHSEL	119	XA15
24	LAD3	56	XA19 /GP17	88	nRI1	120	XD0
25	VCC	57	XA18	89	nDCD1	121	XD1
26	LFRAME#	58	XA17	90	GP50 /nRI2	122	XD2
27	VSS	59	XA16	91	GP51 /nDCD2	123	XD3
28	LDRQ#	60	GP20 /IRRX2 /IRQIN3	92	GP52 /RXD2 /IRRX	124	XD4
29	PCI_RESET#	61	GP21 /IRTX2 /WDT	93	GP53 /TXD2 /IRTX	125	XD5
30	LPCPD#	62	GP22 /IRMODE /IRRX3 /nXCS2	94	GP54 /nDSR2	126	VCC
31	CLKRUN#	63	nINIT	95	GP55 /nRTS2	127	XD6
32	PCI_CLK	64	nSLCTIN	96	GP56 /nCTS2	128	XD7

NOTE: Signals that are mode dependent are shaded gray. These signals are only available when LPC mode is selected.

Table 3.2 - SIO10N268 ISA Mode

PIN #	NAME	PIN #	NAME	PIN #	NAME	PIN #	NAME
1	DRVDEN0	33	SER_IRQ	65	PD0	97	GP57 /nDTR2
2	GP11 /DRVDEN1 /FDC_PP	34	GP30 /nRI3	66	PD1	98	IOCHRDY
3	nMTR0	35	GP31 /nDCD3	67	PD2	99	AEN
4	nDSKCHG	36	GP32 /RXD3	68	PD3	100	nIORD
5	nDS0	37	GP33 /TXD3	69	PD4	101	nIOWR
6	CLOCKI	38	GP34 /nDSR3	70	VCC	102	VCC
7	VSS	39	GP35 /nRTS3	71	PD5	103	SA0
8	nDIR	40	GP36 /nCTS3	72	PD6	104	SA1
9	nSTEP	41	GP37 /nDTR3	73	PD7	105	SA2
10	nWDATA	42	GP40 /nRI4	74	VSS	106	SA3
11	nWGATE	43	GP41 /nDCD4	75	SLCT	107	SA4
12	nHDSEL	44	GP42 /RXD4	76	PE	108	SA5
13	nINDEX	45	GP43 /TXD4	77	BUSY	109	VSS
14	nTRK0	46	GP44 /nDSR4	78	NACK	110	SA6
15	nWRTPRT	47	GP45 /nRTS4	79	NERROR	111	SA7
16	nRDATA	48	GP46 /nCTS4	80	NALF	112	SA8
17	CLKI32	49	VCC	81	NSTROBE	113	SA9
18	nIO_PME	50	GP47 /nDTR4	82	RXD1	114	SA10
19	VTR	51	GP12 /IO_SMI#	83	TXD1	115	SA11
20	GP23 /nLED2 /IRQIN2	52	VSS	84	nDSR1	116	SA12
21	nDACK0	53	GP13 /IRQIN1 /nLED1	85	nRTS1 /SYSOPT	117	SA13
22	nDACK1	54	LPC_ISA	86	nCTS1	118	SA14
23	nDACK2	55	GP16	87	nDTR1	119	SA15
24	nDACK3	56	GP17	88	nRI1	120	SD0
25	VCC	57	TC	89	nDCD1	121	SD1
26	DRQ0	58	DRQ3	90	GP50 /nRI2	122	SD2
27	VSS	59	RESET_DRV	91	GP51 /nDCD2	123	SD3
28	NC	60	GP20 /IRRX2 /IRQIN3	92	GP52 /RXD2 /IRRX	124	SD4
29	DRQ1	61	GP21 /IRTX2 /WDT	93	GP53 /TXD2 /IRTX	125	SD5
30	DRQ2	62	GP22 /IRMODE /IRRX3	94	GP54 /nDSR2	126	VCC
31	NC	63	nINIT	95	GP55 /nRTS2	127	SD6
32	PCI_CLK	64	nSLCTIN	96	GP56 /nCTS2	128	SD7

NOTE: Signals that are mode dependent are shaded gray. These signals are only available when ISA Mode is selected.

Chapter 4 Description of Pin Functions

The following section describes the functionality of the pins for the SIO10N268 in LPC Mode and ISA Mode. The Mode of operation is selected by the LPC_ISA pin. The LPC_ISA pin should be connected directly to VCC to select ISA mode - a pull-up resistor may be used if it is of a low value e.g., 1kohm. It can either be left unconnected or connected to ground to select LPC mode. The pin has a 30uA internal pulldown. Pins or signals that are MODE dependent are shaded gray in the following table.

Table 4.1 - Pin Functions

PIN #	NAME	FUNCTION	BUFFER TYPE (Note 4.1)	POWER WELL
POWER PINS (11)				
25, 49, 70, 102, 126	VCC	+3.3 Volt Supply Voltage (**Note 4.10**)		
19	VTR	+3.3 Volt Standby Supply Voltage (**Note 4.10**)		
7, 27, 52, 74, 109	VSS	Ground		
CLOCK PINS (2)				
17	CLKI32	32.768kHz Standby Clock Input (**Note 4.3**)	IS	VTR
6	CLOCKI	14.318MHz Clock Input	IS	VCC
FDD INTERFACE (14)				
1	DRVDEN0	Drive Density Select 0	O12	VCC
2	GP11 /DRVDEN1 /FDC_PP	General Purpose I/O /Drive Density Select 1 /Floppy on Parallel Port	IO12	VCC (**Note 4.17**)
3	nMTR0	Motor On 0	O12	VCC
4	nDSKCHG	Disk Change	IS	VCC
5	nDS0	Drive Select 0	O12	VCC
8	nDIR	Step Direction	O12	VCC
9	nSTEP	Step Pulse	O12	VCC
10	nWDATA	Write Disk Data	O12	VCC
11	nWGATE	Write Gate	O12	VCC
12	nHDSEL	Head Select	O12	VCC
13	nINDEX	Index Pulse Input	IS	VCC
14	nTRK0	Track 0	IS	VCC
15	nWRTPRT	Write Protected	IS	VCC
16	nRDATA	Read Disk Data	IS	VCC
SERIAL PORT 1 INTERFACE (8)				
82	RXD1	Receive Data 1	IS	VCC

PIN #	NAME	FUNCTION	BUFFER TYPE (Note 4.1)	POWER WELL
83	TXD1	Transmit Data 1	O12	VCC
84	nDSR1	Data Set Ready 1	I	VCC
85	nRTS1 /SYSOPT	Request to Send 1 /(System Option) (**Note 4.6**)	OP14	VCC
86	nCTS1	Clear to Send 1	I	VCC
87	nDTR1 /FWHSEL	Data Terminal Ready 1/(Firmware Hub Select) (**Note 4.16**)	OP14	VCC
88	nRI1	Ring Indicator 1	I	VCC (**Note 4.17**)
89	nDCD1	Data Carrier Detect 1	I	VCC
SERIAL PORT 2 INTERFACE (8)				
90	GP50 /nRI2	General Purpose I/O /Ring Indicator 2	IO8	VCC (**Note 4.17**)
91	GP51 /nDCD2	General Purpose I/O /Data Carrier Detect 2	IO8	VCC
92	GP52 /RXD2 /IRRX	General Purpose I/O /Receive Data 2 /IRRX	IS/O8	VCC
93	GP53 /TXD2 /IRTX	General Purpose I/O /Transmit Data 2 /IRTX (**Note 4.8**, **Note 4.9**)	IO12	VCC
94	GP54 /nDSR2	General Purpose I/O /Data Set Ready 2	IO8	VCC
95	GP55 /nRTS2	General Purpose I/O /Request to Send 2	IO8	VCC
96	GP56 /nCTS2	General Purpose I/O /Clear to Send 2	IO8	VCC
97	GP57 /nDTR2 /MEMEN	General Purpose I/O /Data Terminal Ready 2 /(Memory Enable Option) (**Note 4.15**)	IOP14	VCC
SERIAL PORT 3 INTERFACE (8)				
34	GP30 /nRI3	General Purpose I/O (**Note 4.14**) /Ring Indicator 3	IO8	VCC (**Note 4.17**)
35	GP31 /nDCD3	General Purpose I/O (**Note 4.14**) /Data Carrier Detect 3	IO8	VCC (**Note 4.17**)
SERIAL PORT 3 INTERFACE (8)				
36	GP32 /RXD3	General Purpose I/O (**Note 4.14**) /Receive Data 3	IS/O8	VCC (**Note 4.17**)
37	GP33 /TXD3	General Purpose I/O (**Note 4.14**) /Transmit Data 3	IO12	VCC (**Note 4.17**)

PIN #	NAME	FUNCTION	BUFFER TYPE (Note 4.1)	POWER WELL
38	GP34 /nDSR3	General Purpose I/O (**Note 4.14**) /Data Set Ready 3	IO8	VCC (**Note 4.17**)
39	GP35 /nRTS3	General Purpose I/O (**Note 4.14**) /Request to Send 3	IO8	VCC (**Note 4.17**)
40	GP36 /nCTS3	General Purpose I/O (**Note 4.14**) /Clear to Send 3	IO8	VCC (**Note 4.17**)
41	GP37 /nDTR3	General Purpose I/O (**Note 4.14**) /Data Terminal Ready 3	IO8	VCC (**Note 4.17**)
SERIAL PORT 4 INTERFACE (8)				
42	GP40 /nRI4	General Purpose I/O (**Note 4.14**) /Ring Indicator 4	IO8	VCC (**Note 4.17**)
43	GP41 /nDCD4	General Purpose I/O (**Note 4.14**) /Data Carrier Detect 4	IO8	VCC
44	GP42 /RXD4	General Purpose I/O (**Note 4.14**) /Receive Data 4	IS/O8	VCC
45	GP43 /TXD4	General Purpose I/O (**Note 4.14**) /Transmit Data 4	IO12	VCC
46	GP44 /nDSR4	General Purpose I/O (**Note 4.14**) /Data Set Ready 4	IO8	VCC
47	GP45 /nRTS4	General Purpose I/O (**Note 4.14**) /Request to Send 4	IO8	VCC
48	GP46 /nCTS4	General Purpose I/O (**Note 4.14**) /Clear to Send 4	IO8	VCC
50	GP47 /nDTR4	General Purpose I/O (**Note 4.14**) /Data Terminal Ready 4	IO8	VCC
IR INTERFACE (2)				
60	GP20 /IRRX2 /IRQIN3	General Purpose I/O /IR Receive /IRQ Input 3	IS/O8	VCC (**Note 4.17**)
61	GP21 /IRTX2 /WDT	General Purpose I/O (**Note 4.14**) /IR Transmit (**Note 4.7**, **Note 4.9**) /Watch Dog Timer	IO12	VCC (**Note 4.17**)
PARALLEL PORT INTERFACE (17) (Note 4.4)				
63	nINIT /nDIR	Initiate Output /FDC Direction Control (**Note 4.5**)	OP14	VCC
64	nSLCTIN /nSTEP	Printer Select Input /FDC Step Pulse	OP14	VCC
65	PD0 /nINDEX	Port Data 0 /FDC Index	IOP14/IS	VCC

PIN #	NAME	FUNCTION	BUFFER TYPE (Note 4.1)	POWER WELL
66	PD1 /nTRK0	Port Data 1 /FDC Track 0	IOP14/IS	VCC
67	PD2 /nWRTPRT	Port Data 2 /FDC Write Protected	IOP14/IS	VCC
68	PD3 /nRDATA	Port Data 3 /FDC Read Disk Data	IOP14/IS	VCC
69	PD4 /nDSKCHG	Port Data 4 /FDC Disk Change	IOP14/IS	VCC
71	PD5	Port Data 5	IOP14	VCC
72	PD6 /nMTR0	Port Data 6 /FDC Motor On 0	IOP14 /OD14	VCC
73	PD7	Port Data 7	IOP14	VCC
75	SLCT /nWGATE	Printer Selected Status /FDC Write Gate	IOD12	VCC
76	PE /nWRDATA	Paper End /FDC Write Data	IOD12	VCC
77	BUSY /nMTR1	Busy /FDC Motor On 1	IOD12	VCC
78	nACK /nDS1	Acknowledge /FDC Drive Select 1	IOD12	VCC
79	nERROR /nHDSEL	Error /FDC Head Select	IOD12	VCC
80	nALF /nDRVDEN0	Autofeed Output /FDC Density Select 0 (**Note 4.5**)	OP14	VCC
81	nSTROBE /nDS0	Strobe Output /FDC Drive Select 0 (**Note 4.5**)	OP14	VCC
MISCELLANEOUS GPIO PINS (3)				
51	GP12 /IO_SMI#	General Purpose I/O /System Mgt. Interrupt	IO12	VCC (**Note 4.17**)
53	GP13 /IRQIN1 /nLED1	General Purpose I/O / IRQ Input 1 /nLED1 (**Note 4.11**)	IO12	VCC (**Note 4.17**)
MISCELLANEOUS GPIO PINS (3)				
20	GP23 /nLED2 /IRQIN2	General Purpose I/O /nLED2 (**Note 4.12**) /IRQ Input 2	IO12	VTR (**Note 4.17**)
MODE INDEPENDENT INTERFACE PINS (3)				
18	IO_PME#	Power Management Event Output	O12/OD12	VTR
32	PCI_CLK	PCI Clock	PCI_ICLK	VCC

PIN #	NAME	FUNCTION	BUFFER TYPE (Note 4.1)	POWER WELL
33	SER_IRQ	Serial IRQ	PCI_IO	VCC
MODE CONTROL PIN (1)				
54	LPC_ISA	LPC or ISA device select pin (**Note 4.13**)	IPD	VCC
MODE DEPENDENT INTERFACE PINS				
21	LAD0	Multiplexed Command Address and Data 0	PCI_IO	VCC
22	LAD1	Multiplexed Command Address and Data 1	PCI_IO	VCC
23	LAD2	Multiplexed Command Address and Data 2	PCI_IO	VCC
24	LAD3	Multiplexed Command Address and Data 3	PCI_IO	VCC
26	LFRAME#	Frame	PCI_I	VCC
28	LDRQ#	Encoded DMA Request	PCI_O	VCC
29	PCI_RESET#	PCI Reset	PCI_I	VCC
30	LPCPD#	Power Down (**Note 4.1**)	PCI_I	VCC
31	CLKRUN#	PCI Clock Controller	PCI_OD	VCC
X-BUS PINS (34) – LPC MODE ONLY				
55	XA20 /GP16	X-BUS Address 20 /General Purpose I/O	IO8	VCC (**Note 4.17**)
56	XA19 /GP17	X-BUS Address 19 /General Purpose I/O	IO8	VCC (**Note 4.17**)
57	XA18	X-BUS Address 18	IS/O8	VCC
58	XA17	X-BUS Address 17	O8	VCC
59	XA16	X-BUS Address 16	IS/O8	VCC
62	GP22 /IRMODE /IRRX3 /nXCS2	General Purpose I/O (**Note 4.14**) /IR Mode /IR Receive 3 /X-Bus Chip Select 2	IS/O8	VCC (**Note 4.17**)
98	nXCS0	X-Bus Chip Select 0	O12	VCC
X-BUS PINS (34) – LPC MODE ONLY				
99	nXCS1	X-Bus Chip Select 1	IO8	VCC
100	nXRD	X_BUS Read	IO8	VCC
101	nXWR	X-BUS Write	IO8	VCC
103	XA0	X-BUS Address 0	IO8	VCC
104	XA1	X-BUS Address 1	IO8	VCC
105	XA2	X-BUS Address 2	IO8	VCC
106	XA3	X-BUS Address 3	IO8	VCC
107	XA4	X-BUS Address 4	IO8	VCC
108	XA5	X-BUS Address 5	IO8	VCC

PIN #	NAME	FUNCTION	BUFFER TYPE (Note 4.1)	POWER WELL
110	XA6	X-BUS Address 6	IO8	VCC
111	XA7	X-BUS Address 7	IO8	VCC
112	XA8	X-BUS Address 8	IO8	VCC
113	XA9	X-BUS Address 9	IO8	VCC
114	XA10	X-BUS Address 10	IO8	VCC
115	XA11	X-BUS Address 11	IO8	VCC
116	XA12	X-BUS Address 12	IO8	VCC
117	XA13	X-BUS Address 13	IO8	VCC
118	XA14	X-BUS Address 14	IO8	VCC
119	XA15	X-BUS Address 15	IO8	VCC
120	XD0	X-Bus Data Bit 0	IO12	VCC
121	XD1	X-Bus Data Bit 1	IO12	VCC
X-BUS PINS (34) – LPC MODE ONLY				
122	XD2	X-Bus Data Bit 2	IO12	VCC
123	XD3	X-Bus Data Bit 3	IO12	VCC
124	XD4	X-Bus Data Bit 4	IO12	VCC
125	XD5	X-Bus Data Bit 5	IO12	VCC
127	XD6	X-Bus Data Bit 6	IO12	VCC
128	XD7	X-Bus Data Bit 7	IO12	VCC
ISA INTERFACE (38) – ISA MODE ONLY				
21	nDACK0	DMA Acknowledge 0	PCI_IO	VCC
22	nDACK1	DMA Acknowledge 1	PCI_IO	VCC
23	nDACK2	DMA Acknowledge 2	PCI_IO	VCC
24	nDACK3	DMA Acknowledge 3	PCI_IO	VCC
26	DRQ0	DMA Request 0	O12	VCC
29	DRQ1	DMA Request 1	O12	VCC
30	DRQ2	DMA Request 2	O12	VCC
58	DRQ3	DMA Request 3	O12	VCC
57	TC	Terminal Count	IS/O8	VCC
59	RESET_DRV	ISA Reset Drive	IS/O8	VCC
98	IOCHRDY	I/O Channel Ready	O12	VCC
99	AEN	Address Enable	IO8	VCC
100	nIORD	I/O Read	IO8	VCC
101	nIOWR	I/O Write	IO8	VCC
103	SA0	System Address Bus	IO8	VCC
104	SA1	System Address Bus	IO8	VCC
105	SA2	System Address Bus	IO8	VCC
106	SA3	System Address Bus	IO8	VCC

PIN #	NAME	FUNCTION	BUFFER TYPE (Note 4.1)	POWER WELL
ISA INTERFACE (38) – ISA MODE ONLY				
107	SA4	System Address Bus	IO8	VCC
108	SA5	System Address Bus	IO8	VCC
110	SA6	System Address Bus	IO8	VCC
111	SA7	System Address Bus	IO8	VCC
112	SA8	System Address Bus	IO8	VCC
113	SA9	System Address Bus	IO8	VCC
114	SA10	System Address Bus	IO8	VCC
115	SA11	System Address Bus	IO8	VCC
116	SA12	System Address Bus	IO8	VCC
117	SA13	System Address Bus	IO8	VCC
118	SA14	System Address Bus	IO8	VCC
119	SA15	System Address Bus	IO8	VCC
120	SD0	System Data Bus	IO12	VCC
121	SD1	System Data Bus	IO12	VCC
122	SD2	System Data Bus	IO12	VCC
123	SD3	System Data Bus	IO12	VCC
124	SD4	System Data Bus	IO12	VCC
125	SD5	System Data Bus	IO12	VCC
127	SD6	System Data Bus	IO12	VCC
128	SD7	System Data Bus	IO12	VCC
MISCELLANEOUS MODE DEPENDENT PINS (3) – ISA MODE ONLY				
55	GP16	General Purpose I/O	IO8	VTR (**Note 4.17**)
56	GP17	General Purpose I/O	IO8	VCC
62	GP22 /IRMODE /IRRX3	General Purpose I/O (**Note 4.14**) /IR Mode /IR Receive 3	IS/O8	VCC (**Note 4.17**)

NOTE: The "n" as the first letter of a signal name or the "#" as the suffix of a signal name indicates an "Active Low" signal.

Note 4.1 Pins that have input buffers must always be held to either a logical low or a logical high state when powered. Bi-directional buses that may be tristated should have either weak external pull-ups or pull-downs to prevent the pins from floating.

Note 4.2 The LPCPD# pin may be tied high. The LPC interface will function properly if the PCI_RESET# signal follows the protocol defined for the LRESET# signal in the "Low Pin Count Interface Specification".

Note 4.3 If the 32kHz input clock is not used the CLKI32 pin must be grounded. There is a bit in the configuration register at CR1E that determines whether the 32KHz clock input is used as the clock source for the WDT and the LED's. Set this bit to '1' if the clock is not connected.

Note 4.4 The FDD output pins multiplexed in the PARALLEL PORT INTERFACE are OD drivers only and are not affected by the FDD Output Driver Controls (see subsection CR05 in the Configuration section).

Note 4.5 Active (push-pull) output drivers are required on these pins in the enhanced parallel port modes.

Note 4.6 The nRTS1/SYSOPT pin requires an external pulldown resistor to put the base I/O address for configuration at 0x02E. An external pullup resistor is required to move the base I/O address for configuration to 0x04E.

Note 4.7 The GP21/IRTX2/WDT pin is tristate when VCC=0. The pin comes up as an output and low following a VCC POR and Hard Reset if configured for IRTX2 function. The GP21/IRTX2/WDT pin will remain low following a power-up (VCC POR) if configured for IRTX2 until serial port 2 is enabled by setting the UART2 Power bit to '1'. Once the power has been applied the pin will reflect the state of the IR transmit output of the IRCC block. If this pin is configured for GPIO function, the pin will reflect the state of the GPIO on a VCC POR.

Note 4.8 The GP53/TXD2/IRTX pin defaults to tristate when the part is under VTR power (VCC=0). The pin comes up tristate following a VTR POR, VCC POR, and Hard Reset. If the pin is configured for alternate functions TXD2 or IRTX the GP53/TXD2/IRTX pin will remain tristate following a power-up (VCC POR) until the UART2 Power bit is set to '1'. Once the power has been applied to the UART, the pin will reflect the current state of the output transmit buffer. If this pin is configured for GPIO function, the pin will reflect the state of the GPIO on a VCC POR.

Note 4.9 VTR can be connected to VCC if no wakeup functionality is required.

Note 4.10 VCC must not be greater than 0.5V above VTR.

Note 4.11 The nLED1 pin is powered by VCC and can only be controlled when the part is under VCC power.

Note 4.12 The nLED2 pin is powered by VTR so that the LED can be controlled when the part is under VTR power.

Note 4.13 The LPC_ISA pin should be connected directly to VCC to select ISA mode - a pull-up resistor may be used if it is of a low value e.g., 1kohm. It can either be left unconnected or connected to ground to select LPC mode. The pin has a 30uA internal pulldown.

Note 4.14 These GPIO pins only have push-pull buffers. They cannot be configured for open drain outputs.

Note 4.15 MEMEN is a strapping option to enable/disable memory decoding on the LPC interface for the X-Bus. When MEMEN is asserted (high), the LPC interface will decode memory or FWH addresses for the X-Bus. When MEMEN is deasserted (low), the LPC interface will not decode memory or FWH addresses

Note 4.16 FWHSEL is a strapping option to determine the type of memory cycle decoded when the MEMEN strapping option is asserted. Assuming X-Bus memory cycles are enabled (MEMEN = 1), when FWHSEL is asserted (high) FWH memory cycles are decoded for the X-Bus. When FWHSEL is deasserted (low), LPC memory cycles are decoded for the X-Bus. If MEMEN=0, FWHSEL is has no effect (i.e., Don't Care).

Note 4.17 These pins have input buffers into the wakeup logic that are powered by VTR.

4.1 Buffer Type Description

I	Input TTL Compatible.
IS	Input with Schmitt Trigger.
IPD	Input with 30uA Integrated Pull-Down
O6	Output, 6mA sink, 3mA source.
O8	Output, 8mA sink, 4mA source.
OD8	Open Drain Output, 8mA sink.
IO8	Input/Output, 8mA sink, 4mA source.
O12	Output, 12mA sink, 6mA source.
OD12	Open Drain Output, 12mA sink.
IO12	Input/Output, 12mA sink, 6mA source.
OD14	Open Drain Output, 14mA sink.
OP14	Output, 14mA sink, 14mA source.
IOP14	Input/Output, 14mA sink, 14mA source. Backdrive protected.
PCI_I	Input. These pins meet the PCI 3.3V AC and DC Characteristics. (Note 4.18)
PCI_O	Output. These pins meet the PCI 3.3V AC and DC Characteristics. (Note 4.18)
PCI_OD	Open Drain Output. These pins meet the PCI 3.3V AC and DC Characteristics. (Note 4.18)
PCI_IO	Input/Output. These pins meet the PCI 3.3V AC and DC Characteristics. (Note 4.18)
PCI_ICLK	Clock Input. These pins meet the PCI 3.3V AC and DC Characteristics and timing. (**Note 4.19**)

Note 4.18 See the PCI Local Bus Specification, Revision 2.1, Section 4.2.2.

Note 4.19 See the PCI Local Bus Specification, Revision 2.1, Section 4.2.2. and 4.2.3.

4.2 Design Guidelines for Implemented Buffer Types

The characteristics of the I/O buffers implemented in this device are defined in section 11.2 DC Electrical Characteristics on page 213. Care should be taken to ensure that external devices maintain acceptable voltage levels on all inputs and open drain outputs. It is not advisable to allow input buffers to float or remain in an indeterminate state.

NOTE: It is important not to cross power domains when attaching pull-ups to pins. Pins that are located on the VCC power well must be pulled either to ground or to VCC. This includes GPIO pins with wakeup capability that are located on the VCC power well (see Table 4.1 - Pin Functions on page 18).

Pins that are located on the VTR power well must be pulled either to ground or to VTR.

The following is a list of design guidelines to help identify which pins require external pull-up/pull-down resistors:

1) Input buffers that are of type I or IS must be driven to a logic high or a logic low when power is applied to the buffer. If the external device controlling the input buffer tristates while power is applied to the buffer, an external pull-up/pull-down resistor should be added to prevent the pin from floating.
2) All output pins that are implemented as open drain outputs, must be pulled through an external resistor to the proper VCC or VTR power plane.
3) All GPIO registers default to a GPIO input on a VTR POR. On a cold boot, a VCC POR will implement these pins as GPIO inputs. It is suggested that these pins are pulled to their inactive state (either to the proper VCC or VTR power plane or ground) depending on the function being implemented on the pin.
4) Bi-directional buffers that change direction as part of their functionality require either pull-ups or pull-downs to prevent the input buffer from floating when the bus is tristated. The SIO10N268 has bi-directional data busses that require external resistors pulled to a logic high or a logic low. They are the parallel data pins (PD[0:7]), the X-Bus data pins (XD[0:7]) – LPC Mode only, and ISA data pins (SD[0:7]) – ISA Mode only)

Chapter 5 Block Diagram

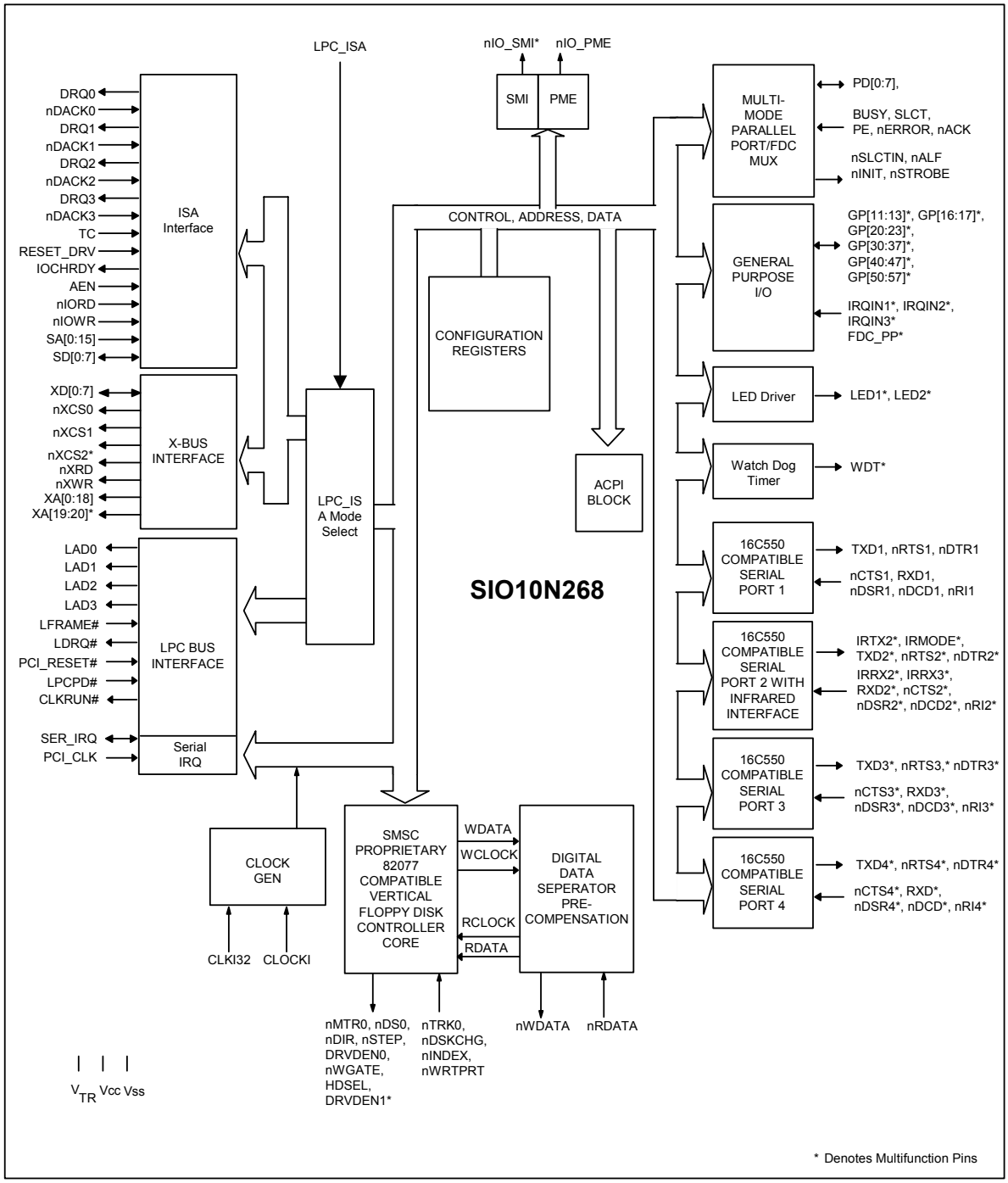


Figure 5.1 - SIO10N268 Block Diagram

Chapter 6 3.3 Volt Operation / 5 Volt Tolerance

The SIO10N268 is a 3.3 Volt part. It is intended solely for 3.3V applications. Non-LPC bus pins are 5V tolerant; that is, the input voltage is 5.5V max, and the I/O buffer output pads are backdrive protected.

The LPC interface pins are 3.3 V only. These signals meet PCI DC specifications for 3.3V signaling. These pins are:

- LAD[3:0]
- LFRAME#
- LDRQ#
- LPCPD#

The input voltage for all other pins is 5.5V max. These pins include all non-LPC Bus pins and the following pins:

- PCI_RESET#
- PCI_CLK
- SER_IRQ
- CLKRUN#
- IO_PME#

Chapter 7 Power Functionality

The SIO10N268 has two power planes: VCC and VTR.

7.1 VCC Power

The SIO10N268 is a 3.3 Volt part. The VCC supply is 3.3 Volts (nominal). See the Operational Description Section and the Maximum Current Values subsection.

7.2 VTR Support

The SIO10N268 requires a trickle supply (V_{TR}) to provide sleep current for the programmable wake-up events in the PME interface when V_{CC} is removed. The VTR supply is 3.3 Volts (nominal). See the Operational Description Section. The maximum VTR current that is required depends on the functions that are used in the part. See Trickle Power Functionality subsection and the Maximum Current Values subsection. If the SIO10N268 is not intended to provide wake-up capabilities on standby current, V_{TR} can be connected to V_{CC}. The V_{TR} pin generates a V_{TR} Power-on-Reset signal to initialize these components.

NOTE: If V_{TR} is to be used for programmable wake-up events when V_{CC} is removed, V_{TR} must be at its full minimum potential at least 10 µs before V_{CC} begins a power-on cycle. When V_{TR} and V_{CC} are fully powered, the potential difference between the two supplies must not exceed 500mV.

7.3 32.768 kHz Trickle Clock Input

The SIO10N268 utilizes a 32.768 kHz trickle input to supply a clock signal for the Watchdog Timer (WDT) and LED blink function.

NOTE: LED1 has a VCC powered output pin and will only generate a signal when the device is powered by VCC. LED2 has a VTR powered output pin and may be used under VTR power.

The SIO10N268 has two different methods of deriving a 32.768kHz signal:

- From an external single-input clock source driven on the CLKI32 pin
- From an internal PLL that divides down the14MHz clock input to make the 32kHz signal

If the 32kHz input clock is not used the CLKI32 pin must be grounded and the CLK32_PRSN bit should be set to ‘1’. This bit in the configuration register block at register index CR1E determines whether the internal 32KHz clock is derived from the CLKI32 pin or the 14MHz clock input. This clock input is used as the clock source for the WDT and the LEDs. This register is powered by VTR and reset on a VTR POR.

Bit[0] (CLK32_PRSN) is defined as follows:

0=32kHz clock is connected to the CLKI32 pin (default)

1=32kHz clock is not connected to the CLKI32 pin (pin is grounded).

Bit 0 controls the source of the 32kHz (nominal) clock for the LED blink logic and the WDT. When the external 32kHz clock is connected, bit[0] should be set to ‘0’ so that the external clock will be the source for the LED blink logic and the WDT. When the external 32kHz clock is not connected, bit[0] should be set to ‘1’ so that an internal 32kHz clock source will be derived from the 14MHz clock for the LED blink logic and the WDT.

The following functions will not work under VTR power (VCC removed) if the external 32kHz clock is not connected. These functions will work under VCC power even if the external 32kHz clock is not connected.

- LED blink
- WDT

7.4 Internal PWRGOOD

An internal PWRGOOD logical control is included to minimize the effects of pin-state uncertainty in the host interface as V_{CC} cycles on and off. When the internal PWRGOOD signal is "1" (active), V_{CC} > 2.3V (nominal), and the SIO10N268 host interface is active. When the internal PWRGOOD signal is "0" (inactive), $V_{CC} \leq$ 2.3V (nominal), and the SIO10N268 host interface is inactive; that is, LPC bus reads and writes will not be decoded.

The SIO10N268 device pins IO_PME#, nRI1, nRI2, nRI3, nRI4, and most GPIOs (as input) are part of the PME interface and remain active when the internal PWRGOOD signal has gone inactive, provided V_{TR} is powered. See Trickle Power Functionality section.

7.5 Trickle Power Functionality

When the SIO10N268 is running under VTR only, the PME wakeup events are active and (if enabled) able to assert the IO_PME# pin active low. The following lists the wakeup events:

- UART 1 Ring Indicator
- UART 2 Ring Indicator
- UART 3 Ring Indicator
- UART 4 Ring Indicator
- WDT
- GPIOs for wakeup. See below.

The following requirements apply to all I/O pins that are specified to be 5 volt tolerant.

- I/O buffers that are wake-up event compatible are powered by VCC. Under VTR power (VCC=0), these pins may only be configured as inputs. These pins have input buffers into the wakeup logic that are powered by VTR.
- I/O buffers that may be configured as either push-pull or open drain under VTR power (VCC=0), are powered by VTR. This means they will, at a minimum, source their specified current from VTR even when VCC is present.

The GPIOs that are used for PME wakeup inputs are GP11-GP13, GP16-GP17, GP20-GP23, GP30-GP37, GP40, and GP50. These GPIOs function as follows:

- Buffers are powered by VCC, but in the absence of VCC they are backdrive protected (they do not impose a load on any external VTR powered circuitry). They are wakeup compatible as inputs under VTR power. These pins have input buffers into the wakeup logic that are powered by VTR.

All GPIOs listed above are for PME wakeup as a GPIO function (or alternate function).

See the Table in the GPIO section for more information.

The following list summarizes the blocks, registers and pins that are powered by VTR.

- PME interface block
- CLKI32
- WDT block

- LED block
- LED2 pin
- Runtime register block (includes all PME, SMI, WDT, LED, and GP data registers)
- Pins for PME Wakeup:
  - GPIOs (GP11-GP13, GP16-GP17, GP20-GP23, GP30-GP37, GP40, and GP50)
  - IO_PME#
  - nRI1, nRI2, nRI3, nRI4

7.6 Maximum Current Values

See Chapter 11 Operational Description for the maximum current values.

The maximum VTR current, I_{TR}, is given with all outputs open (not loaded), and all inputs in a fixed state (i.e., 0V or 3.3V). The total maximum current for the part is the unloaded value PLUS the maximum current sourced by the pin that is driven by VTR. The pins that are powered by VTR (as output) are IO_PME#, LED2 and nPME. These pins, if configured as a push-pull output, will source a minimum of 6mA at 2.4V when driving.

The maximum VCC current, I_{CC}, is given with all outputs open (not loaded), and all inputs in a fixed state (i.e., 0V or 3.3V).

7.7 Power Management Events (PME/SCI)

The SIO10N268 offers support for Power Management Events (PMEs), also referred to as System Control Interrupt (SCI) events. The terms PME and SCI are used synonymously throughout this document to refer to the indication of an event to the chipset via the assertion of the nIO_PME output signal on pin 18. See the “PME Support” section.

Chapter 8 Functional Description

8.1 Super I/O Registers

The address map, shown below in Table 8.1, shows the addresses of the different blocks of the Super I/O immediately after power up. The base addresses of the FDC, serial and parallel ports, runtime register block and configuration register block can be moved via the configuration registers. Some addresses are used to access more than one register.

8.2 Host Processor Interface (LPC or ISA)

The host processor interface is selectable by the LPC_ISA pin (pin 54). The LPC_ISA pin should be connected directly to VCC to select ISA mode - a pull-up resistor should not be used. It can either be left unconnected or connected to ground to select LPC mode. Mode dependent interface pins are shown in the table located in section Chapter 4 Description of Pin Functions on page 18.

The host processor communicates with the SIO10N268 through a series of read/write registers via the host processor interface (LPC or ISA). The port addresses for these registers are shown in Table 8.1. Register access is accomplished through I/O cycles or DMA transfers. All registers are 8 bits wide.

Table 8.1 - Super I/O Block Addresses

ADDRESS	BLOCK NAME	NOTES
Base+(0-5) and +(7)	Floppy Disk	
Base+(0-7)	Serial Port Com 1	
Base1+(0-7) Base2+(0-7)	Serial Port Com 2	IR Support FIR and CIR
Base+(0-7)	Serial Port Com 3	
Base+(0-7)	Serial Port Com 4	
 Base+(0-3) Base+(0-7) Base+(0-3), +(400-402) Base+(0-7), +(400-402)	Parallel Port SPP EPP ECP ECP+EPP+SPP	
Base + (0-F)	Runtime Registers	
Base + (0-1)	Configuration	
 Base +(0) Base +(0)	X-Bus Chip Select 1 (nXCS1) Chip Select 2 (nXCS2)	

Note 8.1 Refer to the configuration register descriptions for setting the base address.

8.3 LPC Interface (LPC Mode only)

LPC Mode is enabled if the LPC_ISA pin (pin 54) is left unconnected of if it is connected to ground.

The SIO10N268 communicates with the host over a Low Pin Count (LPC) interface. For a complete description of the LPC interface, see the Intel Low Pin Count Specification, Rev 1.0. The following sections define the LPC signals implemented, the cycles supported, and protocols implemented that are specific to this device.

NOTE: The LPC interface uses 3.3V signaling. For electrical specifications see the Intel Low Pin Count Specification, Rev 1.0 and the PCI Local Bus Specification, Rev 2.2.

8.3.1 LPC Interface Signal Definition

The signals required for the LPC bus interface are described in the table below. LPC bus signals use PCI 33MHz electrical signal characteristics.

Table 8.2 – LPC Bus Interface Signals

SIGNAL NAME	TYPE	DESCRIPTION
LAD[3:0]	I/O	LPC address/data bus. Multiplexed command, address and data bus.
LFRAME#	Input	Frame signal. Indicates start of new cycle and termination of broken cycle
PCI_RESET#	Input	PCI Reset. Used as LPC Interface Reset.
LDRQ#	Output	Encoded DMA/Bus Master request for the LPC interface.
IO_PME#	OD	Power Mgt Event signal. Allows the SIO10N268 to request wakeup.
LPCPD#	Input	Powerdown Signal. Indicates that the SIO10N268 should prepare for power to be shut on the LPC interface.
PCI_CLK	Input	PCI Clock.
CLKRUN#	I/OD	Clock Run. Allows the SIO10N268 to request the stopped PCI_CLK be started.
IO_SMI#	OD	System Mgt Interrupt signal. Allows the SIO10N268 to notify the host system that an event has occurred.

Note 8.2 The IO_PME#, IO_SMI#, and PCI_CLK signals are considered part of the host interface. They are available in both LPC Mode and ISA Mode.

8.3.2 LPC Cycles

The following cycle types are supported by the LPC protocol.

Table 8.3 – LPC Cycle Types

CYCLE TYPE (Note 8.3)	TRANSFER SIZE
I/O Write	1 Byte
I/O Read	1 Byte
DMA Write	1 Byte
DMA Read	1 Byte
Memory Read	1 Byte (**Note 8.4**, **Note 8.5**)
Memory Write	1 Byte (**Note 8.4**, **Note 8.5**)

Note 8.3 The SIO10N268 ignores cycles that it does not support.

Note 8.4 LPC memory is only supported within the FWH ranges specified in section 8.4.2 FWH and LPC Memory Addressing on page 39.

Note 8.5 LPC Memory transactions are only enabled if the MEM_EN bit is set to '1' and the FWH_SEL bit is set to '0' in the FWH ID Select register.

8.3.3 LFRAME# Usage

LFRAME# is used by the host to indicate the start of cycles and the termination of cycles due to an abort or time-out condition. This signal is to be used by the SIO10N268 to know when to monitor the bus for a cycle.

This signal is used as a general notification that the LAD[3:0] lines contain information relative to the start or stop of a cycle, and that the SIO10N268 monitors the bus to determine whether the cycle is intended for it. The use of LFRAME# allows the SIO10N268 to enter a lower power state internally. There is no need for the SIO10N268 to monitor the bus when it is inactive, so it can decouple its state machines from the bus, and internally gate its clocks.

When the SIO10N268 samples LFRAME# active, it immediately stops driving the LAD[3:0] signal lines on the next clock and monitor the bus for new cycle information.

The LFRAME# signal functions as described in the Low Pin Count (LPC) Interface Specification Revision 1.0.

8.3.4 Field Definitions

LPC transactions are defined as being comprised of multiple fields. These fields may be one or more nibbles in length (nibble=4 bits). All LPC transactions begin with a START field and a Cycle Type/Direction field. The START field is used to initiate/terminate LPC transactions. The Cycle Type/Direction field is used to define the cycle type (memory, I/O, DMA) and direction (read/write) for LPC cycles. The remaining fields of data being transfered are based on specific fields that are used in various combinations, depending on the cycle type. These remaining fields are driven on to the LAD[3:0] signal lines to communicate address, control and data information over the LPC bus between the host and the SIO10N268. See the *Low Pin Count (LPC) Interface Specification* Revision 1.0 from Intel, Section 4.2 for definition of these fields. The following sections describe the supported cycle types.

NOTE: I/O, DMA, and Memory cycles use a START field of 0000.

8.3.4.1 I/O Read and Write Cycles

The SIO10N268 is the target for I/O cycles. I/O cycles are initiated by the host for register or FIFO accesses, and will generally have minimal Sync times. The minimum number of wait-states between bytes is 1. EPP cycles will depend on the speed of the external device, and may have much longer Sync times.

Data transfers are assumed to be exactly 1-byte. If the CPU requested a 16 or 32-bit transfer, the host will break it up into 8-bit transfers.

See the *Low Pin Count (LPC) Interface Specification* Reference, Section 5.2, for the sequence of cycles for the I/O Read and Write cycles.

8.3.4.2 DMA Read and Write Cycles

DMA read cycles involve the transfer of data from the host (main memory) to the SIO10N268. DMA write cycles involve the transfer of data from the SIO10N268 to the host (main memory). Data will be coming from or going to a FIFO and will have minimal Sync times. Data transfers to/from the SIO10N268 are 1 byte.

See the *Low Pin Count (LPC) Interface Specification* Reference, Section 6.4, for the field definitions and the sequence of the DMA Read and Write cycles.

DMA Protocol

DMA on the LPC bus is handled through the use of the LDRQ# lines from the SIO10N268 and special encodings on LAD[3:0] from the host.

The DMA mechanism for the LPC bus is described in the Low Pin Count (LPC) Specification Revision 1.0.

8.3.4.3 Memory Read and Write Cycles

If enabled, the LPC interface is capable of decoding memory cycles that are located in the FWH address ranges specified in section 8.4.2 FWH and LPC Memory Addressing on page 39. To enable LPC memory decoding the MEM_EN bit must be set to '1' and the FWH_SEL bit must be set to '0' in the FWH ID Select register located at offset CR54. The value of these bits is determined on a VCC POR and Hard Reset by the value of the MEM_EN and FWH_SEL strapping options. When VCC>2.4V the MEM_EN and FWH_SEL bits located in the FWH_ID select register can be modified by software. See Table 8.5 - FWH Strapping Options for a description of these strapping options. For a description of the LPC memory read/write cycles refer to section 5.1 Memory Cycles of the LPC Specification.

8.3.5 Power Management

8.3.5.1 CLOCKRUN Protocol

See the Low Pin Count (LPC) Interface Specification Reference, Section 8.1.

8.3.5.2 LPCPD Protocol

The SIO10N268 will function properly if the LPCPD# signal goes active and then inactive again without PCI_RESET# becoming active. This is a requirement for notebook power management functions.

Although the LPC Bus spec 1.0 section 8.2 states, "After LPCPD# goes back inactive, the LPC I/F will always be reset using LRST#", this statement does not apply for mobile systems. LRST# (PCI_RESET#) will not occur if the LPC Bus power was not removed. For example, when exiting a "light" sleep state (ACPI S1, APM POS), LRST# (PCI_RESET#) will not occur. When exiting a "deeper" sleep state (ACPI S3-S5, APM STR, STD, soft-off), LRST# (PCI_RESET#) will occur.

The LPCPD# pin is implemented as a "local" powergood for the LPC bus in the SIO10N268. It is not used as a global powergood for the chip. It is used to reset the LPC block and hold it in reset.

An internal powergood is implemented in SIO10N268 to minimize power dissipation in the entire chip.

Prior to going to a low-power state, the system will assert the LPCPD# signal. It will go active at least 30 microseconds prior to the LCLK# (PCI_CLK) signal stopping low and power being shut to the other LPC I/F signals.

Upon recognizing LPCPD# active, the SIO10N268 will drive the LDRQ# signal low or tri-state, and do so until LPCPD# goes back active.

Upon recognizing LPCPD# inactive, the SIO10N268 will drive its LDRQ# signal high.

See the *Low Pin Count (LPC) Interface Specification* Reference, Section 8.2.

8.3.5.3 SYNC Protocol

See the *Low Pin Count (LPC) Interface Specification* Reference, Section 4.2.1.8 for a table of valid SYNC values.

The SYNC pattern is used to add wait states. For read cycles, the SIO10N268 immediately drives the SYNC pattern upon recognizing the cycle. The host immediately drives the sync pattern for write cycles. If the SIO10N268 needs to assert wait states, it does so by driving 0101 or 0110 on LAD[3:0] until it is ready, at which point it will drive 0000 or 1001. The SIO10N268 will choose to assert 0101 or 0110, but not switch between the two patterns.

The data (or wait state SYNC) will immediately follow the 0000 or 1001 value.

The SYNC value of 0101 is intended to be used for normal wait states, wherein the cycle will complete within a few clocks. The SIO10N268 uses a SYNC of 0101 for all wait states in a DMA transfer.

The SYNC value of 0110 is intended to be used where the number of wait states is large. This is provided for EPP cycles, where the number of wait states could be quite large (>1 microsecond). However, the SIO10N268 uses a SYNC of 0110 for all wait states in an I/O transfer.

The SYNC value is driven within 3 clocks.

8.3.5.4 SYNC Timeout

The SYNC value is driven within 3 clocks. If the host observes 3 consecutive clocks without a valid SYNC pattern, it will abort the cycle.

The SIO10N268 does not assume any particular timeout. When the host is driving SYNC, it may have to insert a very large number of wait states, depending on PCI latencies and retries.

8.3.5.5 SYNC Patterns and Maximum Number of SYNCS

If the SYNC pattern is 0101, then the host assumes that the maximum number of SYNCs is 8.

If the SYNC pattern is 0110, then no maximum number of SYNCs is assumed. The SIO10N268 has protection mechanisms to complete the cycle. This is used for EPP data transfers and will utilize the same timeout protection that is in EPP.

8.3.5.6 SYNC Error Indication

The SIO10N268 reports errors via the LAD[3:0] = 1010 SYNC encoding.

If the host was reading data from the SIO10N268, data will still be transferred in the next two nibbles. This data may be invalid, but it will be transferred by the SIO10N268. If the host was writing data to the SIO10N268, the data had already been transferred.

In the case of multiple byte cycles, such as DMA cycles, an error SYNC terminates the cycle. Therefore, if the host is transferring 4 bytes from a device, if the device returns the error SYNC in the first byte, the other three bytes will not be transferred.

8.3.5.7 Reset Policy

The following rules govern the reset policy:

1) When PCI_RESET# goes inactive (high), the clock is assumed to have been running for 100usec prior to the removal of the reset signal, so that everything is stable. This is the same reset active time after clock is stable that is used for the PCI bus.

2) When PCI_RESET# goes active (low):

   a) the host drives the LFRAME# signal high, tristates the LAD[3:0] signals, and ignores the LDRQ# signal.

   b) the SIO10N268 ignores LFRAME#, tristate the LAD[3:0] pins and drive the LDRQ# signal inactive (high).

8.3.6 LPC Transfers

8.3.6.1 Wait State Requirements

I/O Transfers

For I/O transfers in which long indeterminate wait states are required (i.e., EPP or IrCC transfers) the sync pattern of 0110 is used and a large number of syncs may be inserted (up to 330 which corresponds to a timeout of 10us).

NOTE: Wait states are required for all I/O transfers. Three wait states are required for an I/O read and two wait states are required for an I/O write. A SYNC of 0110 is used for all I/O transfers.

DMA Transfers

The SIO10N268 inserts three wait states for a DMA read and four wait states for a DMA write cycle. A SYNC of 0101 is used for all DMA transfers.

Memory Transfers

For FWH or LPC memory cycles initiated on the LPC interface the number of syncs inserted is dependent on the read/write pulse width programmed for the X-Bus interface. The pulse width is programmed via the CR53 X-Bus chip Select 0 Register which can be found on page 208.

The following table summarizes the number of Long Sync (6\H) clock cycles for LPC and FWH memory transactions.

Table 8.4 – Number of Long Syncs Inserted for Memory Cycles

MIN PULSE WIDTH	LPC MEMORY READ	LPC MEMORY WRITE	FWH READ	FWH WRITE
150 ns	11	7	11	0
120 ns	10	6	10	0
90 ns	9	5	9	0
60 ns	8	4	8	0

Note 8.6 Long sync cycles are always followed by one ready sync cycle (0\H).

See the example timing for the LPC cycles in Chapter 12 Timing Diagrams.

8.4 FWH Interface (LPC Mode Only)

The Firmware Hub (FWH) interface shares the LPC interface pins LAD[3:0] and LFRAME#. The FWH implements a specific memory cycle for the purpose of interface for the BIOS. If enabled, the FWH cycles in the SIO10N268 are forwarded to the X-Bus Interface. To enable FWH memory cycle decoding the MEM_EN bit must be set to '1' and the FWH_SEL bit must be set to '1' in the FWH ID Select register located at offset CR54. The default value of these bits is determined by the MEM_EN and FWH_SEL strapping options. (See Table 8.5 - FWH Strapping Options)

The FWH supports single byte memory transactions only.

8.4.1 Enabling the FWH Interface

The LPC interface can be used to decode FWH memory cycles if enabled. To enable FWH memory cycle decoding the MEM_EN bit must be set to '1' and the FWH_SEL bit must be set to '1' in the FWH ID Select register located at offset CR54. The default value of these bits is determined by the MEM_EN and FWH_SEL strapping options. The following table defines the FWH Strapping options.

Table 8.5 - FWH Strapping Options

	NAME	OPTIONS	PIN	DESCRIPTION
1.	MEMEN	1 = X-Bus Memory Cycles Enabled 0 = X-Bus Memory Cycles Disabled	GP57/nDTR2	When MEMEN is asserted, the LPC interface will decode memory or FWH addresses for the X-Bus. When MEMEN is deasserted, the LPC interface will not decode memory or FWH addresses
2.	FWHSEL	1 = FWH Memory Cycles Selected 0 = LPC Memory Cycles Selected	nDTR1	Assuming X-Bus memory cycles are enabled (MEMEN = 1), when FWHSEL is asserted FWH memory cycles are decoded for the X-Bus. When FWHSEL is deasserted, LPC memory cycles are decoded for the X-Bus.

8.4.1.1 MEMEN

The MEMEN strap option determines if memory cycles are decoded for the X-Bus interface. When the MEMEN strap option is asserted '1' during VCC POR or Hard Reset, the LPC interface will decode LPC or FWH memory cycles (depending on the FWHSEL option). When the MEMEN strap option is deasserted '0' during VCC POR or Hard Reset, the LPC interface will not decode FWH or LPC memory cycles.

The affects of the MEMEN strap option can be overridden by the MEMEN bit in the FWH ID Select register (see section CR54).

8.4.1.2 FWHSEL

The FWHSEL strap option selects whether LPC memory or FWH cycles are decoded for the X-Bus interface, assuming the MEMEN option is asserted.

NOTE: If the MEMEN option is not asserted (MEMEN='0') the FWHSEL bit is a don't care and has no effect on the LPC interface.

When MEMEN = '1' and the FWHSEL strap option is asserted '1' during VCC POR or Hard Reset, the LPC interface will decode FWH cycles for the X-Bus interface. When the MEMEN='1' and the FWHSEL strap option is deasserted '0' during VCC POR or Hard Reset, the LPC interface will decode LPC memory cycles for the X-Bus interface.

The affects of the FWHSEL strap option can be overridden by the FWHSEL bit in the FWH ID Select register. The affects of FWHSEL can also be qualified by the IDSELEN and ID SELECT bits in the FWH ID Select register (see section CR54).

8.4.2 FWH and LPC Memory Addressing

FWH cycles and LPC memory cycles received on the LPC Bus in the following system memory ranges are forwarded to the X-Bus Interface, if enabled. (see Table 8.5 - FWH Strapping Options)

000E0000h to 000FFFFFh – 128KB Legacy BIOS

FF000000h to FFFFFFFFh – 16MB FWH Address Range

NOTE: ICH2 only forwards memory reads/writes to the FWH that are in address ranges 000E0000h to 000FFFFFh and FF000000h to FFFFFFFFh.

If the FWH or LPC memory address is from 000E0000h to 000FFFFFh, address bits 0 – 19 are forwarded to XA0 – XA19 and nXCS0 is enabled. XA20 is driven to '1' to alias the 128KB legacy system BIOS from the top of 1MB to the top of 4GB system memory.

NOTE: At boot-up, all FWH memory cycles will be forwarded to the memory device on chip select 0 (nXCS0 is default) if the MEMEN and FWHSEL strapping options are configured to implement FWH memory transactions.

If the FWH or LPC memory address is from FF000000h to FFFFFFFFh, address bits 0 – 20 are forwarded to XA0 – XA20 and nXCS0 is enabled. The Flash device is aligned with the top 2 MB (FFE00000h – FFFFFFFFh) of the 4 GB system memory space.

NOTE: The full 16MB address space is mapped to the 2MB X-Bus interface, causing aliasing to FWH memory ranges below FFE00000h. Since no address verification is performed on address bit 21-23, the following 2MB address ranges are aliased or mapped to the X-Bus interface: FFC00000h – FFDFFFFFh, FFA00000h – FFBFFFFFh, FF800000h – FF9FFFFFh, FF600000h – FF7FFFFFh, FF400000h – FF5FFFFFh, FF200000h – FF3FFFFFh, and FF000000h – FF1FFFFFh.

8.4.3 FWH Cycle Types

The cycle types supported by the FWH are:

- FWH Memory Read: 1 byte.
- FWH Memory Write: 1 byte.

8.4.4 Field Definitions

8.4.4.1 START

This one clock field indicates the start of a cycle. It is valid on the last clock that FRAME# is sampled low. The two start fields that are used for the cycle are shown in the table below. If the start field that is sampled is not one of these values, then the cycle attempted is not a FWH Memory cycle. It may be a valid memory cycle that the FWH may wish to decode, i.e., it may be of the LPC memory cycle variety.

LAD[3:0]	INDICATION
1101	FWH Memory Read
1110	FWH Memory Write

8.4.4.2 IDSEL

This one clock field is used to indicate which FWH component is being selected. The four bits transmitted over LAD[3:0] during this clock are compared with values strapped onto pins on the FWH component. If there is a match, the FWH component will continue to decode the cycle to determine which bytes are requested on a read or which bytes to update on a write. If there isn't a match, the FWH component may discard the rest of the cycle and go into a standby power state.

8.4.4.3 MSIZE

This one clock field indicates the size of the transfer. This field is fixed to '0000b', other encodings are reserved for future use. A value of '0000b' corresponds to a single byte transfer.

8.4.4.4 MADDR

This is a 7-clock field that gives a 28-bit memory address. This allows for up to 256MB per memory device, for a total of a 4GB addressable space. The address is transferred with the most significant nibble first.

8.4.4.5 SYNC

The SYNC protocol is the same as described in the LPC specification.

8.4.4.6 TAR

The TAR field is the same as described in the LPC specification.

8.4.4.7 Data

The Data field is the same as described in the LPC specification. Data is transferred with the low nibble first.

8.4.5 Protocol

The FWH Memory cycles use a sequence of events that begin with a START field (FRAME# active) with appropriate LAD[3:0] combination, and end with the data transfer. The sections below describe the cycles in detail.

8.4.5.1 Preamble

The FWH Memory transaction begins with the host driving FRAME# low. The 10-clock preamble is then initiated on the LAD[3:0] signals with a START field driven on LAD[3:0] while FRAME# is low. Following the START field is the IDSEL field. The next seven clocks are the 28-bit address from where to begin reading in the selected device. Next, the MSIZE field of 0 indicates 1 byte being transferred in the current transaction.

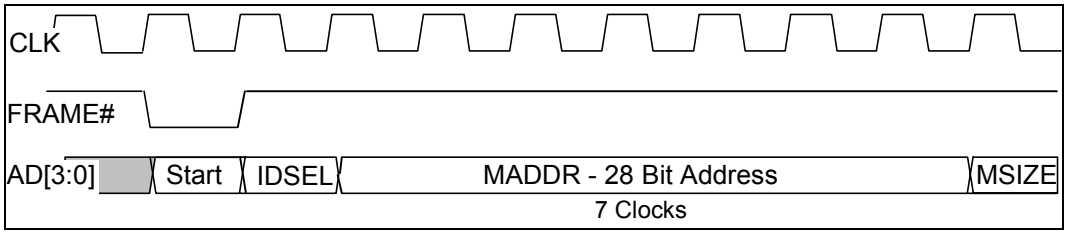


Figure 8.1 - FWH Memory Cycle Preamble

NOTE: Following the preamble, the host drives a TAR field on a read cycle, or drives the low nibble of data on a write cycle. See the following sections for more details.

8.4.6 Read Cycle

8.4.6.1 Single Byte

To indicate that a single byte transfer cycle is being performed, the master asserts an MSIZE value of 0. For read cycles, after the preamble, the host drives a TAR field to give ownership of the bus to the FWH. After the second clock of the TAR phase, the target device assumes the bus and begins driving SYNC values. When it is ready, it drives the low nibble, then the high nibble of data, followed by a TAR to give control back to the host.

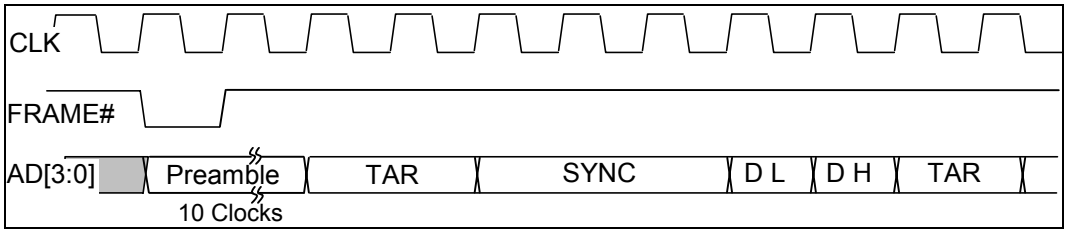


Figure 8.2 - Single Byte Read

Figure 8.2 shows a device that requires 3 SYNC clocks to access data. Since the access time can begin once the address phase has been completed, the two clocks of the TAR phase can be considered as part of the access time of the part. For example, a device with a 120ns access time could assert '0101b' for

clocks 1 and 2 of the SYNC phase and '0000b' for the last clock of the SYNC phase. This would be equivalent to 5 clocks worth of access time if the device started that access at the conclusion of the MADDR phase. Once SYNC is achieved, the device returns the data in two clocks and gives ownership of the bus back to the host with a TAR phase.

8.4.7 Write Cycles

8.4.7.1 Single Byte

All devices that support FWH Memory Write cycles must support single byte writes. FWH Memory Write cycles use the same preamble as FWH Memory read cycles.

To indicate that a single byte transfer cycle is being performed, the master asserts an MSIZE value of 0. After the address and size has been transferred, the 2-clock data phase begins. Following the data phase, bus ownership is transferred to the FWH component with a TAR cycle. Following the TAR phase, the device must assert a SYNC value of '0000b' (ready) or '1010b' (error) indicating the data has been received. Bus ownership is then given back to the master with another TAR phase.

FWH Memory Writes only allow one clock for the SYNC phase. The TAR+SYNC+TAR phases at the end of FWH memory write cycles must be exactly 5 clocks.

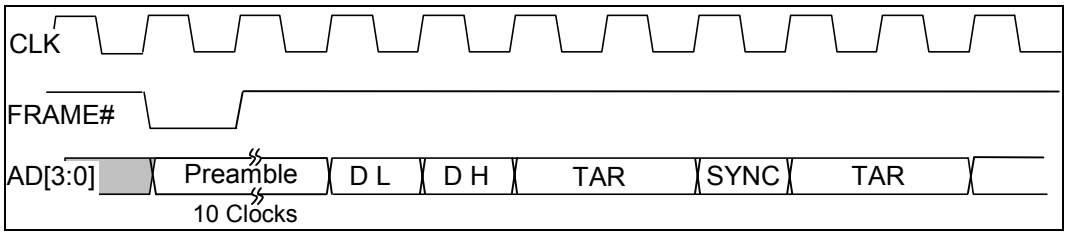


Figure 8.3 - Single Byte Write

8.4.8 Error Reporting

There is no error reporting over the FWH interface for FWH Memory cycles. If an error occurs, such as an address out of range or an unsupported memory size, the cycle will continue from the host unabated. This is because these errors are the result of illegal programming, and there is no efficient error reporting method that can be done to counter the programming error.

Therefore, the FWH component must not report the error conditions over the FWH interface. It must only report wait states and the 'ready' condition. It may choose to log the error internally to be debugged, but it must not signal an error through the FWH interface itself.

8.4.9 FWH Cycle Examples

8.4.9.1 EXAMPLE 1: FWH 1-Byte Read

FIELD	DRIVEN BY	CLOCKS	LAD[3:0]	COMMENT
START	Host	1	1101	LAD[3:0]=1101 (FWH Memory Read)
IDSEL	Host	1	xxxx	LAD[3:0]=selected FWH component
MADDR	Host	1	xxxx	Most significant nibble

FIELD	DRIVEN BY	CLOCKS	LAD[3:0]	COMMENT
MADDR	Host	1	xxxx	.
MADDR	Host	1	xxxx	.
MADDR	Host	1	xxxx	.
MADDR	Host	1	xxxx	.
MADDR	Host	1	xxxx	.
MADDR	Host	1	xxxx	Least significant nibble
MSIZE	Host	1	0000	Number of bytes= 1
TAR	Host	1	1111	Host drives LAD[3:0] high
TAR	Special	1	1111	Not driven
SYNC	Peripheral	1	0101	Sync=0101 (Sync not achieved yet)
SYNC	Peripheral	1	0101	Sync=0101 (Sync not achieved yet)
SYNC	Peripheral	1	0000	Sync=0000 (Sync achieved with no error)
Data	Peripheral	1	xxxx	Least significant nibble of byte
Data	Peripheral	1	xxxx	Most significant nibble of byte
TAR	Peripheral	1	1111	Peripheral drives LAD[3:0] high
TAR	Special	1	1111	Not driven

8.4.9.2 EXAMPLE 2: FWH 1-Byte Write

FIELD	DRIVEN BY	CLOCKS	LAD[3:0]	COMMENT
START	Host	1	1110	LAD[3:0]=1110 (FWH Memory Write)
IDSEL	Host	1	xxxx	LAD[3:0]=selected FWH component
MADDR	Host	1	xxxx	Most significant nibble
MADDR	Host	1	xxxx	.
MADDR	Host	1	xxxx	.
MADDR	Host	1	xxxx	.
MADDR	Host	1	xxxx	.
MADDR	Host	1	xxxx	.
MADDR	Host	1	xxxx	Least significant nibble
MSIZE	Host	1	0000	Number of bytes= 1
Data	Host	1	xxxx	Least significant nibble of byte
Data	Host	1	xxxx	Most significant nibble of byte
TAR	Host	1	1111	Host drives LAD[3:0] high
TAR	Special	1	1111	Not driven
SYNC	Peripheral	1	0000	Sync=0000 (Sync achieved, no errors)
TAR	Peripheral	1	1111	Peripheral drives LAD[3:0] high
TAR	Special	1	1111	Not driven

8.5 X-Bus Interface (LPC Mode Only)

NOTE: The X-Bus interface is only accessible in LPC Mode.

The X-Bus interface is designed to support memory and I/O devices with 21 address pins (XA0–XA20), an 8-bit data bus (XD0 – XD7), and Read and Write signals. This interface offers one chip select to access memory devices (nXCS0) and two chip selects to access I/O devices (nXCS1 and nXCS2). Note that nXCS2 is muxed on the GP22 pin (GP22/IRMODE/IRRX3/nXCS2)

NOTE: It also provides a read strobe (nXRD) and a write strobe (nXWR). These pins default to their inactive state (i.e., inactive state=high) on VCC POR and are tristate when VCC=0V and VTR 3.3V. (These pins must be pulled up to VCC through an external resistor.)

I/O devices located on the X-Bus interface may be accessed by I/O transactions on the LPC interface. Memory or Flash devices located on the X-Bus interface may be accessed by LPC Memory or Firmware Hub (FWH) cycles via the LPC interface. See sections 8.3.4.3 Memory Read and Write Cycles on page 35 and 8.4 FWH Interface (LPC Mode Only) on page 38 for decoding FWH cycles.

NOTE: Chip Select nXCS[0] can be disabled from going active for a memory access by settting the corresponding enable bit to '0', which is located in the X-Bus Chip Select 0 Register. Chip Selects nXCS1and nXCS2 can be disabled from going active for an I/O access by setting the corresponding disable bit to '1', which is located in the associated Base I/O Address x – Low Byte register. These bits allow each chip select to be individually enabled or disabled for either memory or I/O transactions.

8.5.1 I/O Cycles

The X-bus interface allows the SIO10N268 - LPC MODE to interface to as many as 2 external components that have an 8 bit data bus. Devices located on nXCS1 and nXCS2 are accessable by LPC I/O transactions. These devices may have their Base I/O Addresses located on 2, 4, or 16 byte boundaries depending on the X-Bus mode of operation. (See section 10.5 Logical Device Base I/O Address and Range on page 210 for valid Base I/O Addresses for the X-Bus interface.) The SIO10N268 - LPC MODE performs 16-bit address qualification on the X-Bus base I/O addresses. That is, the upper 4-bits, bits[15:12], must be '0'.

The X-Bus interface offers three different modes of operation for I/O devices on both I/O chip selects (nXCS1 and nXCS2). In Mode 1, a 10-bit compare is performed on address bits[11:2] and address bits[1:0] are forwarded to XA1 and XA0 respectively. In Mode 2, an 8-bit compare is performed on address bits[11:4] and address bits[3:0] are forwarded to XA3 to XA0 respectively. In Mode 3, a 10-bit address compare is performed on address bits[11:3] and bits[1] and if address is valid and bit[0]=0 then address bit[2] is forwarded to XA2 .

The chip select outputs are generated by logic that compares the LPC I/O address bits with the X-bus base I/O address configuration registers. The mode of operation determines the number of valid address pins that the X-bus interface provides, as well as the number of bits in the base I/O addresses. The mode is chosen via bits[1:0] of the X-Bus I/O Select Configuration Register located at CR52.

The options for X-bus modes are as follows:

- Mode 1: The X-bus base I/O address configuration registers contain address bits A11 through A8 and A7 through A2, respectively. A1 and A0 pass directly through to XA1 and XA0, respectively. The chip selects only become active (low) for the LPC bus cycle in which the address match occurs.
- Mode 2: The X-bus base I/O address configuration registers contain address bits A11 through A8 and A7 through A4, respectively. A3, A2, A1 and A0 pass directly through to XA3, XA2, XA1 and XA0, respectively. The chip selects only become active (low) for the LPC bus cycle in which the address match occurs.
- Mode 3: The X-bus base I/O address configuration registers contain address bits A11 through A8, A7 though A3, and A1. A2 passes directly through to XA2. A2 is used to select between the registers at base address offset 0 and offset of 4. This mode allows communication with up to three register pairs at a programmable base address and fixed offset of +4, for example (60,64), (62,66), (68,6C). The chip selects only become active (low) for the LPC bus cycle in which the address match occurs. A0 (address bit 0 from LPC bus) must be '0' since registers may only be accessed on even-byte boundaries. That is, only even addresses are valid since the part checks that bit A0 is 0.

Each X-bus chip select base address register has an associated "write protect" bit that can only be set once, and is reset by VCC POR and PCI Reset (i.e., Hard Reset). When this bit is set, it prevents the base address configuration registers (high byte and low byte) for each chip select from being written. This security feature ensures that the base address and disable bit for each chip select can only be set by BIOS

and cannot be corrupted by any virus software. This bit is part of the X-bus Low Address Byte Configuration register.

Each X-bus chip select has an associated disable bit. This bit allows each chip select to be individually enabled or disabled. This bit is part of the X-bus Low Address Byte Configuration register. Setting the disable bit prevents the associated chip select from going active, and prevents the X-bus read and write strobes from going active. In addition, when the disable bit is set, the mode dependent address pins (XA0, XA1, XA2, XA3) will not toggle (they will stay in their previous state). The disable bits default to disabled following a VCC POR and Hard Reset. Once enabled, following a VCC POR, the chip selects are held inactive until a valid LPC I/O cycle results in an address match with the base address register.

The read and write strobes have address setup and hold times, and pulse widths, that are compatible with X-Bus timing of the Intel PIIX4. The strobes will only become active during an LPC cycle in which the LPC address matches the corresponding X-bus address.

8.5.1.1 Conceptual Diagrams of X-Bus I/O interface

The following diagrams are a conceptual diagrams to illustrate the activation of the X-Bus I/O chip selects. It is not intended to indicate the actual implementation.

The following figure shows the X-Bus Interface in mode 1.

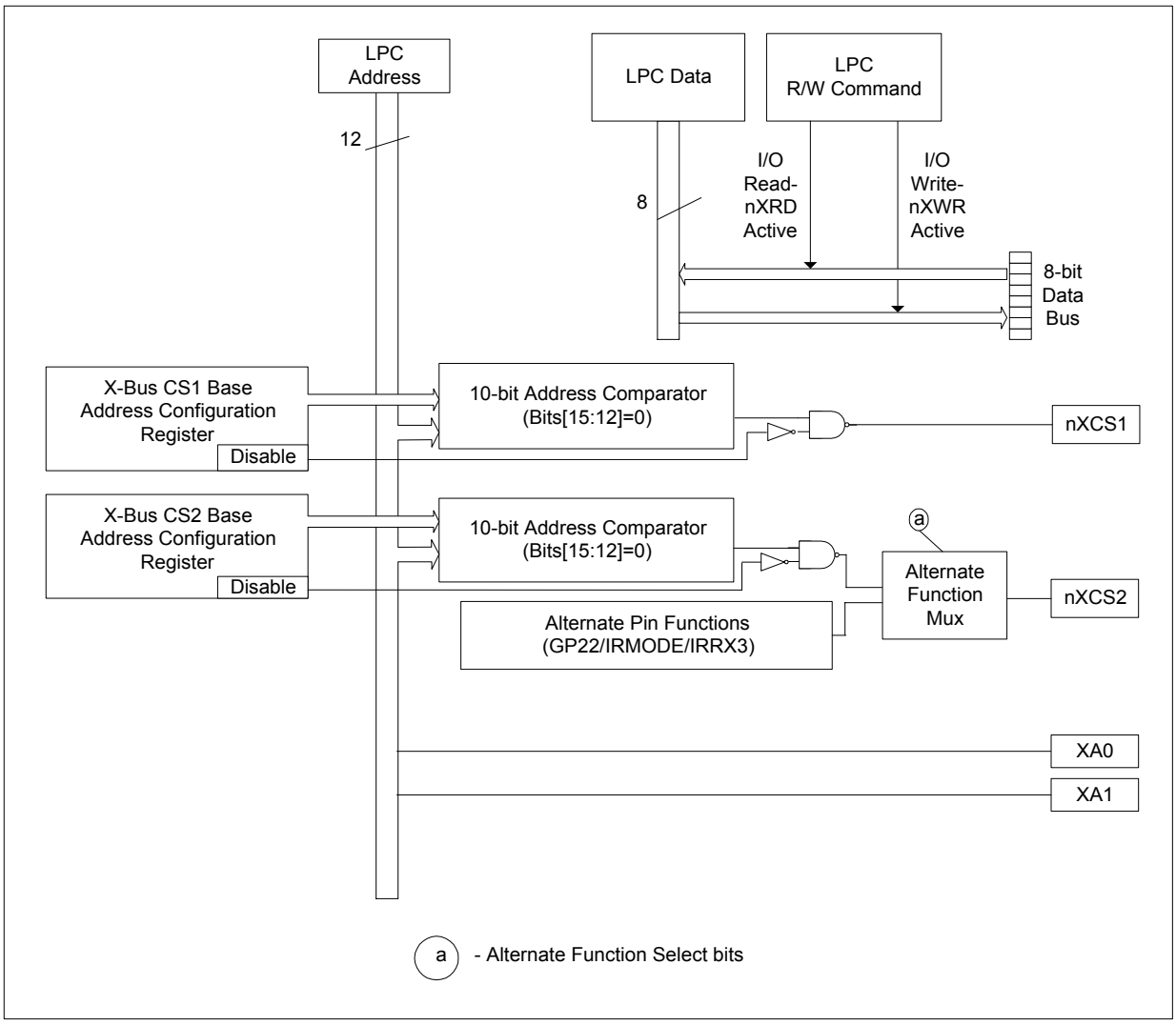


Figure 8.4 - X-Bus Interface, Mode 1

The following figure shows the X-bus interface in mode 2.

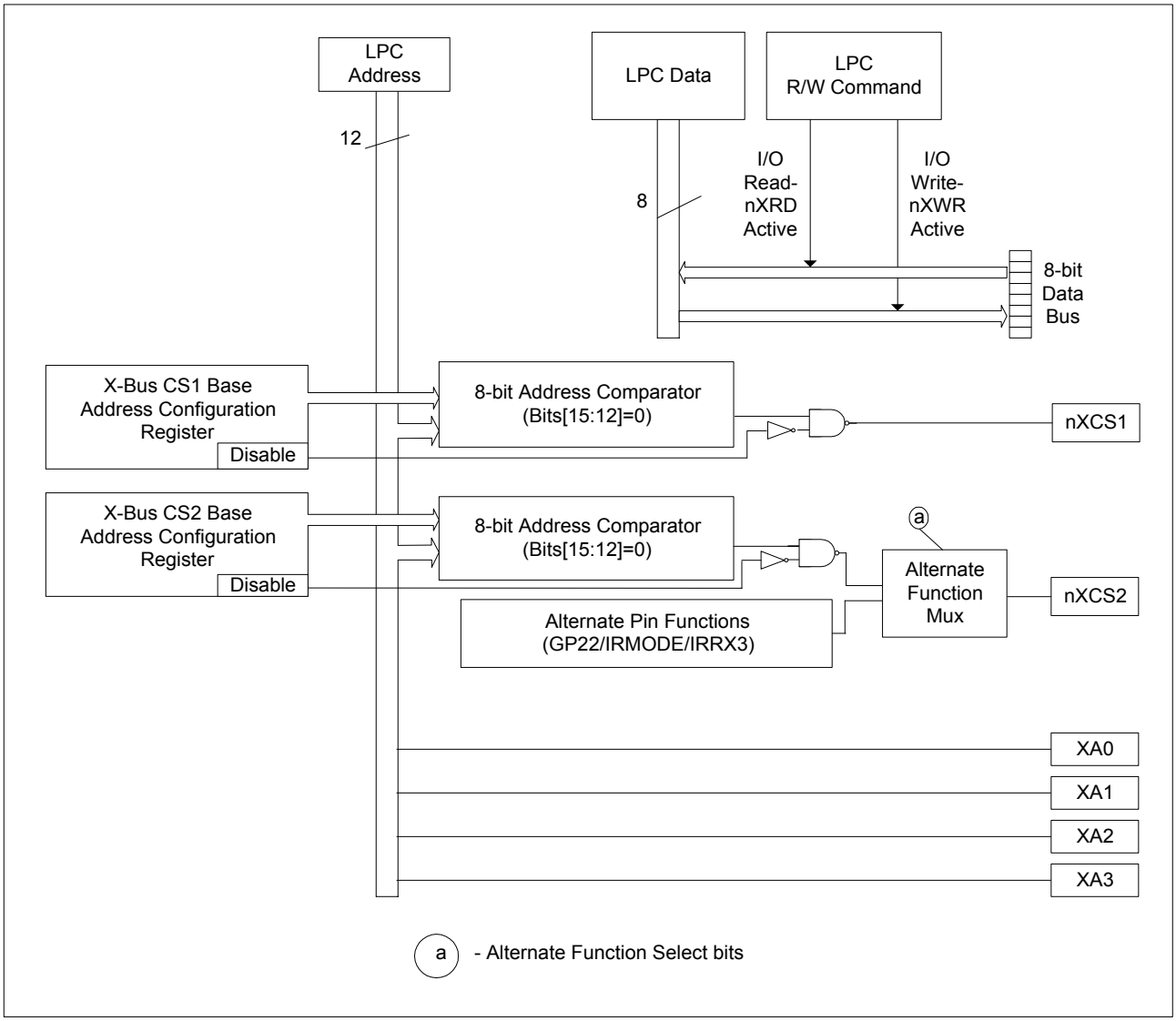


Figure 8.5 - X-Bus Interface, Mode 2

The following figure shows the X-bus interface in mode 3.

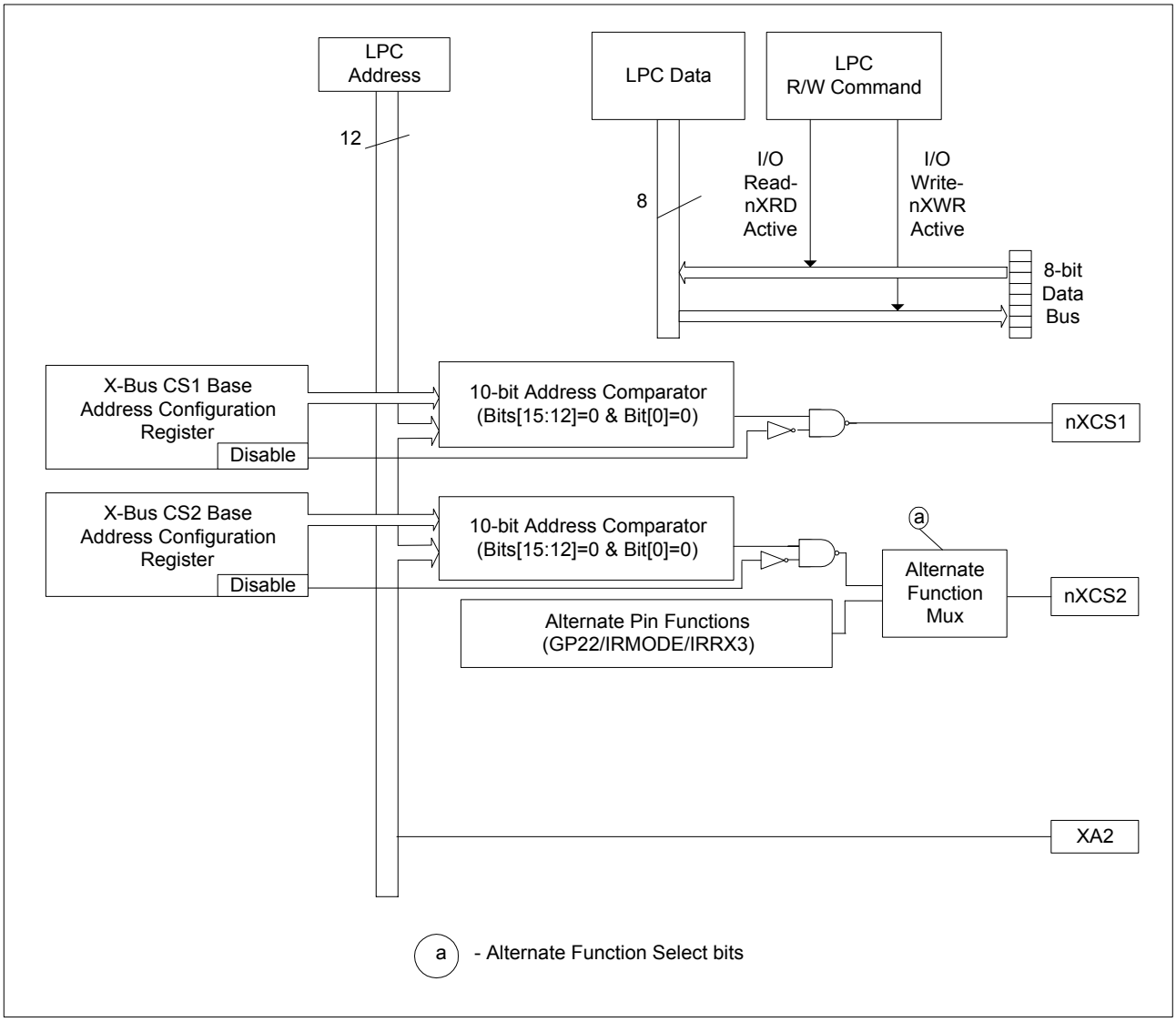


Figure 8.6 - X-Bus Interface, Mode 3

8.5.2 Memory Cycles

All Firmware Hub and LPC memory cycles that have been accepted and decoded by the LPC interface are forwarded to the X-Bus interface and are enabled on nXCS0. See section 8.4.2 FWH and LPC Memory Addressing for a description of the memory cycles forwarded to the X-Bus interface. This interface is capable of accessing up to 2MB (16Mbit) of external flash memory in 8-bit words only.

The X-Bus Chip Select 0 Register at offset CR53 is used to configure access for memory cycles to the X-Bus interface. On a VCC POR and Hard Reset this chip select defaults to be enabled. Chip select 0 (nXCS0) may be disabled by setting bit[7] of the X-Bus Chip Select 0 Register to '0'.

The X-Bus supports flash speed selection by offering a programmable read/write pulse width (see section 12.4.3 X-Bus Memory Cycle Timing on page 225. The read/write pulse width is determined by the Pulse Width Selection bits located in X-Bus Chip Select 0 Register at offset CR53. These bits allow the read/write strobe to be held active for a minimum of 60, 90, 120, or 150 nsec.

The X-Bus Chips Select 0 Register offers a write protect bit. This bit affords the BIOS the ability to program CR53 for a particular configuration, which cannot be altered until a VCC POR or Hard Reset.

NOTE: To tristate the X-Bus for production line Flash update put the device in XNOR chain test mode.

8.6 ISA Interface (ISA Mode Only)

ISA Mode is enabled by pulling pin 54 (LPC_ISA) directly to VCC – a pull-up resistor should not be used.

The ISA interface is a standard AT (Advanced Technology) interface, that is compatible with the ISA (Industry Standard Architecture) as documented by IEEE (IEEE P996 compatible). This interface supports I/O and DMA transactions as defined by this defacto standard. In addition this interface has been modified to have the option of supporting ISA devices that do not have an AEN output signal (Devices like the Intel 440MX chipset). The following sections define the signals on the ISA interface and the modifications made to support special chipsets like the 440MX.

NOTE: For ISA timing see section 12.5 Host Timing (ISA Mode Only) on page 227.

Table 8.6 - Description of ISA Signals

NAME	SYMBOL	DESCRIPTION
System Data Bus 0-7	SD0-SD7	The system data bus connection used by the host microprocessor to transmit data to and from the chip. These pins are in a high-impedance state when not in the output mode.
I/O Read	nIORD	This active low signal is issued by the host microprocessor to indicate an I/O read operation.
I/O Write	nIOWR	This active low signal is issued by the host microprocessor to indicate an I/O write operation.
Address Enable	AEN	Active high Address Enable indicates DMA operations on the host data bus. Used internally to qualify appropriate address decodes. (See section 8.6.1 AEN signal following table.)
System Address Bus	SA0-SA15	These host address bits determine the I/O address to be accessed during nIOR and nIOW cycles. These bits are latched internally by the leading edge of nIOR and nIOW. All internal address decodes use the full A0 to A15 address bits.
DMA Request 0, 1, 2, 3	DRQ_0 DRQ_1 DRQ_2 DRQ_3	These active high outputs are the DMA request for byte transfers of data between the host and the chip. These signals are cleared on the last byte of the data transfer by the nDACK signal going low (or by nIOR going low if nDACK was already low as in demand mode).
nDMA Acknowl-edge 0, 1, 2, 3	nDACK_0 nDACK_1 nDACK_2 nDACK_3	These are active low inputs acknowledging the request for a DMA transfer of data between the host and the chip. These inputs enable the DMA read or write internally.
Terminal Count	TC	This signal indicates that DMA data transfer is complete. TC is only accepted when nDACK_x is low. In AT and PS/2 model 30 modes, TC is active high and in PS/2 mode, TC is active low.
Serial IRQ	SER_IRQ	Serial IRQ pin used with the PCI_CLK pin to transfer SIO10N268 interrupts to the host.

NAME	SYMBOL	DESCRIPTION
PCI Clock	PCI_CLK	33MHz PCI clock input, used with the SIRQ and the CLKRUN# pins to serially transfer SIO10N268 interrupts to the host.
ISA Reset Drive	RESET_DRV	This active high signal resets the chip and must be valid for 500ns minimum. The effect on the internal registers is described in the appropriate section. The configuration registers are not affected by this reset.
I/O Channel Ready (**Note 8.7**)	IOCHRDY	This pin is pulled low to extend the read/write command. IOCHRDY can be used by the IRCC and by the Parallel Port in EPP mode.
Power Management Event	IO_PME#	Power Mgt Event signal. Allows the SIO10N268 to request wakeup.
System Management Event	IO_SMI#	System Mgt Interrupt signal. Allows the SIO10N268 to notify the host system that an event has occurred.

Note 8.7 An external pull-up must be provided for IOCHRDY.

The SER_IRQ, PCI_CLK, IO_PME#, and IO_SMI# signals are considered part of the host interface. They are available in both LPC Mode and ISA Mode.

8.6.1 AEN signal

The AEN signal is used to indicate that a DMA operation is active on the host bus. It is used to prevent I/O devices from responding to DMA transactions. Not all devices that provide an ISA interface support this feature. For example, the 440MX chipset does not supply an AEN signal, instead it drives the address bus to 0000h during a DMA I/O cycle to indicate a DMA transaction is occuring. The SIO10N268 has implemented two modes of operation that are selectable via the AEN control bit located in the Clock/AEN Control Register located at offset CR1E. This bit is implemented as shown.

bit[1] AEN Control

1) If the AEN Control bit is set to '0' the internal AEN signal will be asserted if the AEN pin is high OR if SA[0:15]=0000h (default).
2) If the AEN Control bit is set to '1' the internal AEN signal will asserted only when the AEN pin is high.

NOTE: System designers using the 440MX chipset should ground the AEN pin to prevent the AEN pin from floating, thereby creating false DMA cycles.

The SIO10N268 only responds to I/O addresses above 100h.

8.7 Floppy Disk Controller

The Floppy Disk Controller (FDC) provides the interface between a host microprocessor and the floppy disk drives. The FDC integrates the functions of the Formatter/Controller, Digital Data Separator, Write Precompensation and Data Rate Selection logic for an IBM XT/AT compatible FDC. The true CMOS 765B core guarantees 100% IBM PC XT/AT compatibility in addition to providing data overflow and underflow protection.

The FDC is compatible to the 82077AA using SMSC's proprietary floppy disk controller core.

The SIO10N268 supports one floppy disk drive directly through the FDC interface pins and two floppy disk drives the FDC interface on the parallel port pins. It can also be configured to support on drive on the FDC interface pins and one drive on the parallel port pins.

8.7.1 FDC Internal Registers

The Floppy Disk Controller contains eight internal registers that facilitate the interfacing between the host microprocessor and the disk drive. Table 8.7 shows the addresses required to access these registers. Registers other than the ones shown are not supported. The rest of the description assumes that the primary addresses have been selected.

Table 8.7 – Status, Data and Control Registers

(Shown with base addresses of 3F0 and 370)

PRIMARY ADDRESS	SECONDARY ADDRESS	R/W	REGISTER
3F0	370	R	Status Register A (SRA)
3F1	371	R	Status Register B (SRB)
3F2	372	R/W	Digital Output Register (DOR)
3F3	373	R/W	Tape Drive Register (TDR)
3F4	374	R	Main Status Register (MSR)
3F4	374	W	Data Rate Select Register (DSR)
3F5	375	R/W	Data (FIFO)
3F6	376		Reserved
3F7	377	R	Digital Input Register (DIR)
3F7	377	W	Configuration Control Register (CCR)

8.7.1.1 Status Register A (SRA)

Address 3F0 READ ONLY

This register is read-only and monitors the state of the internal interrupt signal and several disk interface pins in PS/2 and Model 30 modes. The SRA can be accessed at any time when in PS/2 mode. In the PC/AT mode the data bus pins D0 - D7 are held in a high impedance state for a read of address 3F0.

PS/2 Mode

	7	6	5	4	3	2	1	0
	INT PENDING	nDRV2	STEP	nTRK0	HDSEL	nINDEX	nWP	DIR
RESET COND.	0	1	0	N/A	0	N/A	N/A	0

BIT 0 DIRECTION

Active high status indicating the direction of head movement. A logic "1" indicates inward direction; a logic "0" indicates outward direction.

BIT 1 nWRITE PROTECT

Active low status of the WRITE PROTECT disk interface input. A logic "0" indicates that the disk is write protected.

BIT 2 nINDEX

Active low status of the INDEX disk interface input.

BIT 3 HEAD SELECT

Active high status of the HDSEL disk interface input. A logic "1" selects side 1 and a logic "0" selects side 0.

BIT 4 nTRACK 0

Active low status of the TRK0 disk interface input.

BIT 5 STEP

Active high status of the STEP output disk interface output pin.

BIT 6 nDRV2

This function is not supported. This bit is always read as “1”.

BIT 7 INTERRUPT PENDING

Active high bit indicating the state of the Floppy Disk Interrupt output.

PS/2 Model 30 Mode

	7	6	5	4	3	2	1	0
	INT PENDING	DRQ	STEP F/F	TRK0	nHDSEL	INDEX	WP	nDIR
RESET COND.	0	0	0	N/A	1	N/A	N/A	1

BIT 0 nDIRECTION

Active low status indicating the direction of head movement. A logic "0" indicates inward direction; a logic "1" indicates outward direction.

BIT 1 WRITE PROTECT

Active high status of the WRITE PROTECT disk interface input. A logic "1" indicates that the disk is write protected.

BIT 2 INDEX

Active high status of the INDEX disk interface input.

BIT 3 nHEAD SELECT

Active low status of the HDSEL disk interface input. A logic "0" selects side 1 and a logic "1" selects side 0.

BIT 4 TRACK 0

Active high status of the TRK0 disk interface input.

BIT 5 STEP

Active high status of the latched STEP disk interface output pin. This bit is latched with the STEP output going active, and is cleared with a read from the DIR register, or with a hardware or software reset.

BIT 6 DMA REQUEST

Active high status of the DMA request pending.

BIT 7 INTERRUPT PENDING

Active high bit indicating the state of the Floppy Disk Interrupt.

8.7.1.2 Status Register B (SRB)

Address 3F1 READ ONLY

This register is read-only and monitors the state of several disk interface pins in PS/2 and model 30 modes. The SRB can be accessed at any time when in PS/2 mode. In the PC/AT mode the data bus pins D0 - D7 are held in a high impedance state for a read of address 3F1.

PS/2 Mode

	7	6	5	4	3	2	1	0
	1	1	DRIVE SEL0	WDATA TOGGLE	RDATA TOGGLE	WGATE	MOT EN1	MOT EN0
RESET COND.	1	1	0	0	0	0	0	0

BIT 0 MOTOR ENABLE 0

Active high status of the MTR0 disk interface output pin. This bit is low after a hardware reset and unaffected by a software reset.

BIT 1 MOTOR ENABLE 1

Active high status of the MTR1 disk interface output pin. This bit is low after a hardware reset and unaffected by a software reset.

BIT 2 WRITE GATE

Active high status of the WGATE disk interface output.

BIT 3 READ DATA TOGGLE

Every inactive edge of the RDATA input causes this bit to change state.

BIT 4 WRITE DATA TOGGLE

Every inactive edge of the WDATA input causes this bit to change state.

BIT 5 DRIVE SELECT 0

Reflects the status of the Drive Select 0 bit of the DOR (address 3F2 bit 0). This bit is cleared after a hardware reset and it is unaffected by a software reset.

BIT 6 RESERVED

Always read as a logic "1".

BIT 7 RESERVED

Always read as a logic "1".

PS/2 Model 30 Mode

	7	6	5	4	3	2	1	0
	nDRV2	nDS1	nDS0	WDATA F/F	RDATA F/F	WGATE F/F	nDS3	nDS2
RESET COND.	N/A	1	1	0	0	0	1	1

BIT 0 nDRIVE SELECT 2

The DS2 disk interface is not supported.

BIT 1 nDRIVE SELECT 3

The DS3 disk interface is not supported.

BIT 2 WRITE GATE

Active high status of the latched WGATE output signal. This bit is latched by the active going edge of WGATE and is cleared by the read of the DIR register.

BIT 3 READ DATA

Active high status of the latched RDATA output signal. This bit is latched by the inactive going edge of RDATA and is cleared by the read of the DIR register.

BIT 4 WRITE DATA

Active high status of the latched WDATA output signal. This bit is latched by the inactive going edge of WDATA and is cleared by the read of the DIR register. This bit is not gated with WGATE.

BIT 5 nDRIVE SELECT 0

Active low status of the DS0 disk interface output.

BIT 6 nDRIVE SELECT 1

Active low status of the DS1 disk interface output.

BIT 7 nDRV2

Active low status of the DRV2 disk interface input. Note: This function is not supported.

8.7.1.3 Digital Output Register (DOR)

Address 3F2 READ/WRITE

The DOR controls the drive select and motor enables of the disk interface outputs. It also contains the enable for the DMA logic and a software reset bit. The contents of the DOR are unaffected by a software reset. The DOR can be written to at any time.

	7	6	5	4	3	2	1	0
	MOT EN3	MOT EN2	MOT EN1	MOT EN0	DMAEN	nRESET	DRIVE SEL1	DRIVE SEL0
RESET COND.	0	0	0	0	0	0	0	0

BIT 0 and 1 DRIVE SELECT

These two bits are binary encoded for the drive selects, thereby allowing only one drive to be selected at one time.

BIT 2 nRESET

A logic "0" written to this bit resets the Floppy disk controller. This reset will remain active until a logic "1" is written to this bit. This software reset does not affect the DSR and CCR registers, nor does it affect the other bits of the DOR register. The minimum reset duration required is 100ns, therefore toggling this bit by consecutive writes to this register is a valid method of issuing a software reset.

BIT 3 DMAEN

PC/AT and Model 30 Mode: Writing this bit to logic "1" will enable the DMA and interrupt functions. This bit being a logic "0" will disable the DMA and interrupt functions. This bit is a logic "0" after a reset and in these modes.

PS/2 Mode: In this mode the DMA and interrupt functions are always enabled. During a reset, this bit will be cleared to a logic "0".

BIT 4 MOTOR ENABLE 0

This bit controls the MTR0 disk interface output. A logic "1" in this bit will cause the output pin to go active.

BIT 5 MOTOR ENABLE 1

This bit controls the MTR1 disk interface output. A logic "1" in this bit will cause the output pin to go active.

BIT 6 MOTOR ENABLE 2

The MTR2 disk interface output is not supported.

BIT 7 MOTOR ENABLE 3

The MTR3 disk interface output is not supported.

DRIVE	DOR VALUE
0	1CH
1	2DH

Table 8.8 - Internal 2 Drive Decode (Normal)

DIGITAL OUTPUT REGISTER				DRIVE SELECT OUTPUTS (ACTIVE LOW)		MOTOR ON OUTPUTS (ACTIVE LOW)	
Bit 5	Bit 4	Bit1	Bit 0	nDS1	nDS0	nMTR1	nMTR0
X	1	0	0	1	0	nBIT 5	nBIT 4
1	X	0	1	0	1	nBIT 5	nBIT 4
0	0	X	X	1	1	nBIT 5	nBIT 4

Table 8.9 - Internal 2 Drive Decode (Drives 0 and 1 Swapped)

DIGITAL OUTPUT REGISTER				DRIVE SELECT OUTPUTS (ACTIVE LOW)		MOTOR ON OUTPUTS (ACTIVE LOW)	
Bit 5	Bit 4	Bit1	Bit 0	nDS1	nDS0	nMTR1	nMTR0
X	1	0	0	0	1	nBIT 4	nBIT 5
1	X	0	1	1	0	nBIT 4	nBIT 5
0	0	X	X	1	1	nBIT 4	nBIT 5

8.7.1.4 Tape Drive Register (TDR)

Address 3F3 READ/WRITE

The Tape Drive Register (TDR) is included for 82077 software compatibility and allows the user to assign tape support to a particular drive during initialization. Any future references to that drive automatically invokes tape support. The TDR Tape Select bits TDR.[1:0] determine the tape drive number. Table 8.10 illustrates the Tape Select Bit encoding. Note that drive 0 is the boot device and cannot be assigned tape support. The remaining Tape Drive Register bits TDR.[7:2] are tristated when read. The TDR is unaffected by a software reset.

Table 8.10 - Tape Select Bits

TAPE SEL1 (TDR.1)	TAPE SEL0 (TDR.0)	DRIVE SELECTED
0	0	None
0	1	1
1	0	2
1	1	3

Note 8.8 The SIO10N268 supports one floppy drive directly on the FDC interface pins and two floppy drives on the Parallel Port.

Normal Floppy Mode

Normal mode. Register 3F3 contains only bits 0 and 1. When this register is read, bits 2 - 7 are '0'.

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
REG 3F3	0	0	0	0	0	0	tape sel1	tape sel0

Enhanced Floppy Mode 2 (OS2)

Register 3F3 for Enhanced Floppy Mode 2 operation.

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
REG 3F3	Reserved	Reserved	Drive Type ID		Floppy Boot Drive		tape sel1	tape sel0

Table 8.11 - Drive Type ID

DIGITAL OUTPUT REGISTER		REGISTER 3F3 - DRIVE TYPE ID	
Bit 1	Bit 0	Bit 5	Bit 4
0	0	CR06 - B1	CR06 - B0
0	1	CR06 - B3	CR06 - B2
1	0	CR06 - B5	CR06 - B4
1	1	CR06 - B7	CR06 - B6

Note 8.9 CR06-Bx = Configuration Register 06, Bit x.

8.7.1.5 Data Rate Select Register (DSR)

Address 3F4 WRITE ONLY

This register is write only. It is used to program the data rate, amount of write precompensation, power down status, and software reset. The data rate is programmed using the Configuration Control Register (CCR) not the DSR, for PC/AT and PS/2 Model 30 applications. Other applications can set the data rate in the DSR. The data rate of the floppy controller is the most recent write of either the DSR or CCR. The DSR is unaffected by a software reset. A hardware reset will set the DSR to 02H, which corresponds to the default precompensation setting and 250 Kbps.

	7	6	5	4	3	2	1	0
	S/W RESET	POWER DOWN	0	PRE-COMP2	PRE-COMP1	PRE-COMP0	DRATE SEL1	DRATE SEL0
RESET COND.	0	0	0	0	0	0	1	0

BIT 0 and 1 DATA RATE SELECT

These bits control the data rate of the floppy controller. See Table 8.13 for the settings corresponding to the individual data rates. The data rate select bits are unaffected by a software reset, and are set to 250 Kbps after a hardware reset.

BIT 2 through 4 PRECOMPENSATION SELECT

These three bits select the value of write precompensation that will be applied to the WDATA output signal. Table 8.12 shows the precompensation values for the combination of these bits settings. Track 0 is the

default starting track number to start precompensation. This starting track number can be changed by the configure command.

BIT 5 UNDEFINED

Should be written as a logic "0".

BIT 6 LOW POWER

A logic "1" written to this bit will put the floppy controller into manual low power mode. The floppy controller clock and data separator circuits will be turned off. The controller will come out of manual low power mode after a software reset or access to the Data Register or Main Status Register.

BIT 7 SOFTWARE RESET

This active high bit has the same function as the DOR RESET (DOR bit 2) except that this bit is self clearing.

NOTE: The DSR is Shadowed in the Floppy Data Rate Select Shadow Register, located in the Configuration section (CR14).

Table 8.12 - Precompensation Delays

PRECOMP 432	PRECOMPENSATION DELAY (nsec)	
	<2Mbps	2Mbps
111	0.00	0
001	41.67	20.8
010	83.34	41.7
011	125.00	62.5
100	166.67	83.3
101	208.33	104.2
110	250.00	125
000	Default	Default

Default: See Table 8.15

Table 8.13 - Data Rates

DRIVE RATE		DATA RATE		DATA RATE		DENSEL	DRATE(1)	
DRT1	DRT0	SEL1	SEL0	MFM	FM		1	0
0	0	1	1	1Meg	---	1	1	1
0	0	0	0	500	250	1	0	0
0	0	0	1	300	150	0	0	1
0	0	1	0	250	125	0	1	0
0	1	1	1	1Meg	---	1	1	1
0	1	0	0	500	250	1	0	0
0	1	0	1	500	250	0	0	1
0	1	1	0	250	125	0	1	0
1	0	1	1	1Meg	---	1	1	1
1	0	0	0	500	250	1	0	0
1	0	0	1	2Meg	---	0	0	1

1	0	1	0	250	125	0	1	0

Drive Rate Table (Recommended) 00 = 360K, 1.2M, 720K, 1.44M and 2.88M Vertical Format

01 = 3-Mode Drive

10 = 2 Meg Tape

Note 8.10 The DRATE and DENSEL values are mapped onto the DRVDEN pins.

Table 8.14 - DRVDEN Mapping0

DT1	DT0	DRVDEN1 (1)	DRVDEN0 (1)	DRIVE TYPE
0	0	DRATE0	DENSEL	4/2/1 MB 3.5" 2/1 MB 5.25" FDDS 2/1.6/1 MB 3.5" (3-MODE)
1	0	DRATE0	DRATE1	
0	1	DRATE0	nDENSEL	PS/2
1	1	DRATE1	DRATE0	

Table 8.15 – Default Precompensation Delays

DATA RATE	PRECOMPENSATION DELAYS
2 Mbps	20.8 ns
1 Mbps	41.67 ns
500 Kbps	125 ns
300 Kbps	125 ns
250 Kbps	125 ns

8.7.1.6 Main Status Register (MSR)

Address 3F4 READ ONLY

The Main Status Register is a read-only register and indicates the status of the disk controller. The Main Status Register can be read at any time. The MSR indicates when the disk controller is ready to receive data via the Data Register. It should be read before each byte transferring to or from the data register except in DMA mode. No delay is required when reading the MSR after a data transfer.

7	6	5	4	3	2	1	0
RQM	DIO	NON DMA	CMD BUSY	Reserved	Reserved	DRV1 BUSY	DRV0 BUSY

BIT 0 1 DRV x BUSY

These bits are set to 1s when a drive is in the seek portion of a command, including implied and overlapped seeks and recalibrates.

BIT 4 COMMAND BUSY

This bit is set to a 1 when a command is in progress. This bit will go active after the command byte has been accepted and goes inactive at the end of the results phase. If there is no result phase (Seek, Recalibrate commands), this bit is returned to a 0 after the last command byte.

BIT 5 NON-DMA

Reserved, read '0'. This part does not support non-DMA mode.

BIT 6 DIO

Indicates the direction of a data transfer once a RQM is set. A 1 indicates a read and a 0 indicates a write is required.

BIT 7 RQM

Indicates that the host can transfer data if set to a 1. No access is permitted if set to a 0.

8.7.1.7 Data Register (FIFO)

Address 3F5 READ/WRITE

All command parameter information, disk data and result status are transferred between the host processor and the floppy disk controller through the Data Register.

Data transfers are governed by the RQM and DIO bits in the Main Status Register.

The Data Register defaults to FIFO disabled mode after any form of reset. This maintains PC/AT hardware compatibility. The default values can be changed through the Configure command (enable full FIFO operation with threshold control). The advantage of the FIFO is that it allows the system a larger DMA latency without causing a disk error. Table 8.16 gives several examples of the delays with a FIFO.

The data is based upon the following formula:

$$\text{Threshold \# x} \left| \frac{1}{\text{DATA RATE}} \times 8 \right| - 1.5\ \mu s = \text{DELAY}$$

At the start of a command, the FIFO action is always disabled and command parameters are sent based upon the RQM and DIO bit settings. As the command execution phase is entered, the FIFO is cleared of any data to ensure that invalid data is not transferred.

An overrun or underrun will terminate the current command and the transfer of data. Disk writes will complete the current sector by generating a 00 pattern and valid CRC. Reads require the host to remove the remaining data so that the result phase may be entered.

Table 8.16 - FIFO Service Delay

FIFO THRESHOLD EXAMPLES	MAXIMUM DELAY TO SERVICING AT 2 Mbps DATA RATE
1 byte	1 x 4 µs - 1.5 µs = 2.5 µs
2 bytes	2 x 4 µs - 1.5 µs = 6.5 µs
8 bytes	8 x 4 µs - 1.5 µs = 30.5 µs
15 bytes	15 x 4 µs - 1.5 µs = 58.5 µs

FIFO THRESHOLD EXAMPLES	MAXIMUM DELAY TO SERVICING AT 1 Mbps DATA RATE
1 byte	1 x 8 µs - 1.5 µs = 6.5 µs
2 bytes	2 x 8 µs - 1.5 µs = 14.5 µs
8 bytes	8 x 8 µs - 1.5 µs = 62.5 µs
15 bytes	15 x 8 µs - 1.5 µs = 118.5 µs

FIFO THRESHOLD EXAMPLES	MAXIMUM DELAY TO SERVICING AT 500 Kbps DATA RATE
1 byte	1 x 16 µs - 1.5 µs = 14.5 µs
2 bytes	2 x 16 µs - 1.5 µs = 30.5 µs
8 bytes	8 x 16 µs - 1.5 µs = 126.5 µs
15 bytes	15 x 16 µs - 1.5 µs = 238.5 µs

8.7.1.8 Digital Input Register (DIR)

Address 3F7 READ ONLY

This register is read-only in all modes.

PC-AT Mode

	7	6	5	4	3	2	1	0
	DSK CHG	0	0	0	0	0	0	0
RESET COND.	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

BIT 0 - 6 UNDEFINED

The data bus outputs D0 - 6 are read as '0'.

BIT 7 DSKCHG

This bit monitors the pin of the same name and reflects the opposite value seen on the disk cable or the value programmed in the Force FDD Status Change Register (CR17). see the Configuration section for register description.

PS/2 Mode

	7	6	5	4	3	2	1	0
	DSK CHG	1	1	1	1	DRATE SEL1	DRATE SEL0	nHIGH nDENS
RESET COND.	N/A	N/A	N/A	N/A	N/A	N/A	N/A	1

BIT 0 nHIGH DENS

This bit is low whenever the 500 Kbps or 1 Mbps data rates are selected, and high when 250 Kbps and 300 Kbps are selected.

BITS 1 - 2 DATA RATE SELECT

These bits control the data rate of the floppy controller. See Table 8.13 for the settings corresponding to the individual data rates. The data rate select bits are unaffected by a software reset, and are set to 250 Kbps after a hardware reset.

BITS 3 - 6 UNDEFINED

Always read as a logic "1"

BIT 7 DSKCHG

This bit monitors the pin of the same name and reflects the opposite value seen on the disk cable or the value programmed in the Force Disk Change Register (CR17). See the Configuration section for register description.

Model 30 Mode

	7	6	5	4	3	2	1	0
	DSK CHG	0	0	0	DMAEN	NOPREC	DRATE SEL1	DRATE SEL0
RESET COND.	N/A	0	0	0	0	0	1	0

BITS 0 - 1 DATA RATE SELECT

These bits control the data rate of the floppy controller. See Table 8.13 for the settings corresponding to the individual data rates. The data rate select bits are unaffected by a software reset, and are set to 250 Kbps after a hardware reset.

BIT 2 NOPREC

This bit reflects the value of NOPREC bit set in the CCR register.

BIT 3 DMAEN

This bit reflects the value of DMAEN bit set in the DOR register bit 3.

BITS 4 - 6 UNDEFINED

Always read as a logic "0"

BIT 7 DSKCHG

This bit monitors the pin of the same name and reflects the opposite value seen on the disk cable or the value programmed in the Force Disk Change Register (CR17). See the Configuration section for register description.

8.7.1.9 Configuration Control Register (CCR)

Address 3F7 WRITE ONLY

PC/AT and PS/2 Modes

	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	DRATE SEL1	DRATE SEL0
RESET COND.	N/A	N/A	N/A	N/A	N/A	N/A	1	0

BIT 0 and 1 DATA RATE SELECT 0 and 1

These bits determine the data rate of the floppy controller. See Table 8.13 for the appropriate values.

BIT 2 - 7 RESERVED

Should be set to a logical "0".

PS/2 Model 30 Mode

	7	6	5	4	3	2	1	0
	0	0	0	0	0	NOPREC	DRATE SEL1	DRATE SEL0
RESET COND.	N/A	N/A	N/A	N/A	N/A	N/A	1	0

BIT 0 and 1 DATA RATE SELECT 0 and 1

These bits determine the data rate of the floppy controller. See Table 8.13 for the appropriate values.

BIT 2 NO PRECOMPENSATION

This bit can be set by software, but it has no functionality. It can be read by bit 2 of the DSR when in Model 30 register mode. Unaffected by software reset.

BIT 3 - 7 RESERVED

Should be set to a logical "0"

Table 8.14 shows the state of the DENSEL pin. The DENSEL pin is set high after a hardware reset and is unaffected by the DOR and the DSR resets.

8.7.2 Status Register Encoding

During the Result Phase of certain commands, the Data Register contains data bytes that give the status of the command just executed.

Table 8.17 - Status Register 0

BIT NO.	SYMBOL	NAME	DESCRIPTION
7,6	IC	Interrupt Code	00 - Normal termination of command. The specified command was properly executed and completed without error. 01 - Abnormal termination of command. Command execution was started, but was not successfully completed. 10 - Invalid command. The requested command could not be executed. 11 - Abnormal termination caused by Polling.
5	SE	Seek End	The FDC completed a Seek, Relative Seek or Recalibrate command (used during a Sense Interrupt Command).
4	EC	Equipment Check	The TRK0 pin failed to become a "1" after: 1. 255 step pulses in the Recalibrate command. 2. The Relative Seek command caused the FDC to step outward beyond Track 0.

BIT NO.	SYMBOL	NAME	DESCRIPTION
3			Unused. This bit is always "0".
2	H	Head Address	The current head address.
1,0	DS1,0	Drive Select	The current selected drive.

Table 8.18 - Status Register 1

BIT NO.	SYMBOL	NAME	DESCRIPTION
7	EN	End of Cylinder	The FDC tried to access a sector beyond the final sector of the track (255D). Will be set if TC is not issued after Read or Write Data command.
6			Unused. This bit is always "0".
5	DE	Data Error	The FDC detected a CRC error in either the ID field or the data field of a sector.
4	OR	Overrun/ Underrun	Becomes set if the FDC does not receive CPU or DMA service within the required time interval, resulting in data overrun or underrun.
3			Unused. This bit is always "0".
2	ND	No Data	Any one of the following: 1. Read Data, Read Deleted Data command - the FDC did not find the specified sector. 2. Read ID command - the FDC cannot read the ID field without an error. 3. Read A Track command - the FDC cannot find the proper sector sequence.
1	NW	Not Writeable	WP pin became a "1" while the FDC is executing a Write Data, Write Deleted Data, or Format A Track command.
0	MA	Missing Address Mark	Any one of the following: 1. The FDC did not detect an ID address mark at the specified track after encountering the index pulse from the nINDEX pin twice. 2. The FDC cannot detect a data address mark or a deleted data address mark on the specified track.

Table 8.19 - Status Register 2

BIT NO.	SYMBOL	NAME	DESCRIPTION
7			Unused. This bit is always "0".
6	CM	Control Mark	Any one of the following: Read Data command - the FDC encountered a deleted data address mark. Read Deleted Data command - the FDC encountered a data address mark.
5	DD	Data Error in Data Field	The FDC detected a CRC error in the data field.
4	WC	Wrong Cylinder	The track address from the sector ID field is different from the track address maintained inside the FDC.
3			Unused. This bit is always "0".
2			Unused. This bit is always "0".
1	BC	Bad Cylinder	The track address from the sector ID field is different from the track address maintained inside the FDC and is equal to FF hex, which indicates a bad track with a hard error according to the IBM soft-sectored format.

BIT NO.	SYMBOL	NAME	DESCRIPTION
0	MD	Missing Data Address Mark	The FDC cannot detect a data address mark or a deleted data address mark.

Table 8.20 - Status Register 3

BIT NO.	SYMBOL	NAME	DESCRIPTION
7			Unused. This bit is always "0".
6	WP	Write Protected	Indicates the status of the WRTPRT pin.
5			Unused. This bit is always "1".
4	T0	Track 0	Indicates the status of the TRK0 pin.
3			Unused. This bit is always "1".
2	HD	Head Address	Indicates the status of the HDSEL pin.
1,0	DS1,0	Drive Select	Indicates the status of the DS1, DS0 pins.

8.7.2.1 Reset

There are three sources of system reset on the FDC: the PCI_RESET# pin, a reset generated via a bit in the DOR, and a reset generated via a bit in the DSR. At power on, a Power On Reset initializes the FDC. All resets take the FDC out of the power down state.

All operations are terminated upon a PCI_RESET#, and the FDC enters an idle state. A reset while a disk write is in progress will corrupt the data and CRC.

On exiting the reset state, various internal registers are cleared, including the Configure command information, and the FDC waits for a new command. Drive polling will start unless disabled by a new Configure command.

PCI_RESET# Pin (Hardware Reset)

The PCI_RESET# pin is a global reset and clears all registers except those programmed by the Specify command. The DOR reset bit is enabled and must be cleared by the host to exit the reset state.

DOR Reset vs. DSR Reset (Software Reset)

These two resets are functionally the same. Both will reset the FDC core, which affects drive status information and the FIFO circuits. The DSR reset clears itself automatically while the DOR reset requires the host to manually clear it. DOR reset has precedence over the DSR reset. The DOR reset is set automatically upon a pin reset. The user must manually clear this reset bit in the DOR to exit the reset state.

8.7.2.2 Modes Of Operation

The FDC has three modes of operation, PC/AT mode, PS/2 mode and Model 30 mode. These are determined by the state of the Interface Mode bits (MFM and IDENT) in CR03[5,6].

PC/AT mode

The PC/AT register set is enabled, the DMA enable bit of the DOR becomes valid (controls the interrupt and DMA functions), and DENSEL is an active high signal.

PS/2 mode

This mode supports the PS/2 models 50/60/80 configuration and register set. The DMA bit of the DOR becomes a "don't care". The DMA and interrupt functions are always enabled, and DENSEL is active low.

Model 30 mode

This mode supports PS/2 Model 30 configuration and register set. The DMA enable bit of the DOR becomes valid (controls the interrupt and DMA functions), and DENSEL is active low.

8.7.3 DMA Transfers

DMA transfers are enabled with the Specify command and are initiated by the FDC by activating a DMA request cycle. DMA read, write and verify cycles are supported. The FDC supports two DMA transfer modes: single Transfer and Burst Transfer. Burst mode is enabled via CR05-Bit[2]. See the Configuration section.

8.7.4 Controller Phases

For simplicity, command handling in the FDC can be divided into three phases: Command, Execution, and Result. Each phase is described in the following sections.

8.7.4.1 Command Phase

After a reset, the FDC enters the command phase and is ready to accept a command from the host. For each of the commands, a defined set of command code bytes and parameter bytes has to be written to the FDC before the command phase is complete. (Please refer to Table 8.21 for the command set descriptions). These bytes of data must be transferred in the order prescribed.

Before writing to the FDC, the host must examine the RQM and DIO bits of the Main Status Register. RQM and DIO must be equal to "1" and "0" respectively before command bytes may be written. RQM is set false by the FDC after each write cycle until the received byte is processed. The FDC asserts RQM again to request each parameter byte of the command unless an illegal command condition is detected. After the last parameter byte is received, RQM remains "0" and the FDC automatically enters the next phase as defined by the command definition.

The FIFO is disabled during the command phase to provide for the proper handling of the "Invalid Command" condition.

8.7.4.2 Execution Phase

All data transfers to or from the FDC occur during the execution phase, which can proceed in DMA or non-DMA mode as indicated in the Specify command.

After a reset, the FIFO is disabled. Each data byte is transferred by a read/write or DMA cycle depending on the DMA mode. The Configure command can enable the FIFO and set the FIFO threshold value.

The following paragraphs detail the operation of the FIFO flow control. In these descriptions, <threshold> is defined as the number of bytes available to the FDC when service is requested from the host and ranges from 1 to 16. The parameter FIFOTHR, which the user programs, is one less and ranges from 0 to 15.

A low threshold value (i.e. 2) results in longer periods of time between service requests, but requires faster servicing of the request for both read and write cases. The host reads (writes) from (to) the FIFO until

empty (full), then the transfer request goes inactive. The host must be very responsive to the service request. This is the desired case for use with a "fast" system.

A high value of threshold (i.e. 12) is used with a "sluggish" system by affording a long latency period after a service request, but results in more frequent service requests.

Non-DMA Mode - Transfers from the FIFO to the Host

This part does not support non-DMA mode.

Non-DMA Mode - Transfers from the Host to the FIFO

This part does not support non-DMA mode.

DMA Mode - Transfers from the FIFO to the Host

The FDC generates a DMA request cycle when the FIFO contains (16 - <threshold>) bytes, or the last byte of a full sector transfer has been placed in the FIFO. The DMA controller responds to the request by reading data from the FIFO. The FDC will deactivate the DMA request when the FIFO becomes empty by generating the proper sync for the data transfer.

DMA Mode - Transfers from the Host to the FIFO.

The FDC generates a DMA request cycle when entering the execution phase of the data transfer commands. The DMA controller responds by placing data in the FIFO. The DMA request remains active until the FIFO becomes full. The DMA request cycle is reasserted when the FIFO has <threshold> bytes remaining in the FIFO. The FDC will terminate the DMA cycle after a TC, indicating that no more data is required.

8.7.4.3 Data Transfer Termination

The FDC supports terminal count explicitly through the TC cycle and implicitly through the underrun/overrun and end-of-track (EOT) functions. For full sector transfers, the EOT parameter can define the last sector to be transferred in a single or multi-sector transfer.

If the last sector to be transferred is a partial sector, the host can stop transferring the data in mid-sector, and the FDC will continue to complete the sector as if a TC cycle was received. The only difference between these implicit functions and TC cycle is that they return "abnormal termination" result status. Such status indications can be ignored if they were expected.

NOTE: When the host is sending data to the FIFO of the FDC, the internal sector count will be complete when the FDC reads the last byte from its side of the FIFO. There may be a delay in the removal of the transfer request signal of up to the time taken for the FDC to read the last 16 bytes from the FIFO. The host must tolerate this delay.

8.7.4.4 Result Phase

The generation of the interrupt determines the beginning of the result phase. For each of the commands, a defined set of result bytes has to be read from the FDC before the result phase is complete. These bytes of data must be read out for another command to start.

RQM and DIO must both equal "1" before the result bytes may be read. After all the result bytes have been read, the RQM and DIO bits switch to "1" and "0" respectively, and the CB bit is cleared, indicating that the FDC is ready to accept the next command.

8.7.5 Command Set/Descriptions

Commands can be written whenever the FDC is in the command phase. Each command has a unique set of needed parameters and status results. The FDC checks to see that the first byte is a valid command and, if valid, proceeds with the command. If it is invalid, an interrupt is issued. The user sends a Sense Interrupt Status command which returns an invalid command error. Refer to Table 8.21 for explanations of the various symbols used. Table 8.22 lists the required parameters and the results associated with each command that the FDC is capable of performing.

Table 8.21 - Description of Command Symbols

SYMBOL	NAME	DESCRIPTION
C	Cylinder Address	The currently selected address; 0 to 255.
D	Data Pattern	The pattern to be written in each sector data field during formatting.
D0, D1	Drive Select 0-1	Designates which drives are perpendicular drives on the Perpendicular Mode Command. A "1" indicates a perpendicular drive.
DIR	Direction Control	If this bit is 0, then the head will step out from the spindle during a relative seek. If set to a 1, the head will step in toward the spindle.
DS0, DS1	Disk Drive Select	DS1 DS0 DRIVE 0 0 Drive 0 0 1 Drive 1
DTL	Special Sector Size	By setting N to zero (00), DTL may be used to control the number of bytes transferred in disk read/write commands. The sector size (N = 0) is set to 128. If the actual sector (on the diskette) is larger than DTL, the remainder of the actual sector is read but is not passed to the host during read commands; during write commands, the remainder of the actual sector is written with all zero bytes. The CRC check code is calculated with the actual sector. When N is not zero, DTL has no meaning and should be set to FF HEX.
EC	Enable Count	When this bit is "1" the "DTL" parameter of the Verify command becomes SC (number of sectors per track).
EFIFO	Enable FIFO	This active low bit when a 0, enables the FIFO. A "1" disables the FIFO (default).
EIS	Enable Implied Seek	When set, a seek operation will be performed before executing any read or write command that requires the C parameter in the command phase. A "0" disables the implied seek.
EOT	End of Track	The final sector number of the current track.
GAP		Alters Gap 2 length when using Perpendicular Mode.
GPL	Gap Length	The Gap 3 size. (Gap 3 is the space between sectors excluding the VCO synchronization field).
H/HDS	Head Address	Selected head: 0 or 1 (disk side 0 or 1) as encoded in the sector ID field.
HLT	Head Load Time	The time interval that FDC waits after loading the head and before initializing a read or write operation. Refer to the Specify command for actual delays.
HUT	Head Unload Time	The time interval from the end of the execution phase (of a read or write command) until the head is unloaded. Refer to the Specify command for actual delays.
LOCK		Lock defines whether EFIFO, FIFOTHR, and PRETRK parameters of the CONFIGURE COMMAND can be reset to their default values by a "software Reset". (A reset caused by writing to the appropriate bits of either the DSR or DOR)
MFM	MFM/FM Mode Selector	A one selects the double density (MFM) mode. A zero selects single density (FM) mode.

SYMBOL	NAME	DESCRIPTION
MT	Multi-Track Selector	When set, this flag selects the multi-track operating mode. In this mode, the FDC treats a complete cylinder under head 0 and 1 as a single track. The FDC operates as this expanded track started at the first sector under head 0 and ended at the last sector under head 1. With this flag set, a multitrack read or write operation will automatically continue to the first sector under head 1 when the FDC finishes operating on the last sector under head 0.
N	Sector Size Code	This specifies the number of bytes in a sector. If this parameter is "00", then the sector size is 128 bytes. The number of bytes transferred is determined by the DTL parameter. Otherwise the sector size is (2 raised to the "N'th" power) times 128. All values up to "07" hex are allowable. "07"h would equal a sector size of 16k. It is the user's responsibility to not select combinations that are not possible with the drive. N SECTOR SIZE 00 128 Bytes 01 256 Bytes 02 512 Bytes 03 1024 Bytes … … 07 16K Bytes
NCN	New Cylinder Number	The desired cylinder number.
ND	Non-DMA Mode Flag	Write '0'. This part does not support non-DMA mode.
OW	Overwrite	The bits D0-D3 of the Perpendicular Mode Command can only be modified if OW is set to 1. OW id defined in the Lock command.
PCN	Present Cylinder Number	The current position of the head at the completion of Sense Interrupt Status command.
POLL	Polling Disable	When set, the internal polling routine is disabled. When clear, polling is enabled.
PRETRK	Precompensation Start Track Number	Programmable from track 00 to FFH.
R	Sector Address	The sector number to be read or written. In multi-sector transfers, this parameter specifies the sector number of the first sector to be read or written.
RCN	Relative Cylinder Number	Relative cylinder offset from present cylinder as used by the Relative Seek command.
SC	Number of Sectors Per Track	The number of sectors per track to be initialized by the Format command. The number of sectors per track to be verified during a Verify command when EC is set.
SK	Skip Flag	When set to 1, sectors containing a deleted data address mark will automatically be skipped during the execution of Read Data. If Read Deleted is executed, only sectors with a deleted address mark will be accessed. When set to "0", the sector is read or written the same as the read and write commands.
SRT	Step Rate Interval	The time interval between step pulses issued by the FDC. Programmable from 0.5 to 8 milliseconds in increments of 0.5 ms at the 1 Mbit data rate. Refer to the SPECIFY command for actual delays.

SYMBOL	NAME	DESCRIPTION
ST0 ST1 ST2 ST3	Status 0 Status 1 Status 2 Status 3	Registers within the FDC which store status information after a command has been executed. This status information is available to the host during the result phase after command execution.
WGATE	Write Gate	Alters timing of WE to allow for pre-erase loads in perpendicular drives.

8.7.6 Instruction Set

Table 8.22 - Instruction Set

READ DATA										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	0	0	1	1	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information prior to Command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and system.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

READ DELETED DATA										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	0	1	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information prior to Command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and system.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

WRITE DATA										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	0	0	0	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information prior to Command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and system.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

WRITE DELETED DATA										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	0	0	1	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information prior to Command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and system.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

READ A TRACK										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	0	0	1	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information prior to Command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and system. FDC reads all of cylinders' contents from index hole to EOT.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

VERIFY										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	1	0	1	1	0	Command Codes
	W	EC	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information prior to Command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL/SC								
Execution										No data transfer takes place.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

VERSION										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	0	0	Command Code
Result	R	1	0	0	1	0	0	0	0	Enhanced Controller

FORMAT A TRACK										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	1	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	N								Bytes/Sector
	W	SC								Sectors/Cylinder
	W	GPL								Gap 3
	W	D								Filler Byte
Execution for	W	C								Input Sector Parameters

FORMAT A TRACK										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Each Sector Repeat:										
	W	H								
	W	R								
	W	N								
										FDC formats an entire cylinder
Result	R	ST0								Status information after Command execution
	R	ST1								
	R	ST2								
	R	Undefined								
	R	Undefined								
	R	Undefined								
	R	Undefined								

RECALIBRATE									
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	1	1	1	Command Codes
	W	0	0	0	0	0	0	DS1	DS0	
Execution										Head retracted to Track 0 Interrupt.

SENSE INTERRUPT STATUS										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	0	0	0	Command Codes
Result	R	ST0								Status information at the end of each seek operation.
	R	PCN								

SPECIFY										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	0	1	1	Command Codes
	W	SRT				HUT				
	W	HLT							ND	

SENSE DRIVE STATUS										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
Result	R	ST3								Status information about FDD

SEEK										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	1	1	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	NCN								
Execution										Head positioned over proper cylinder on diskette.

CONFIGURE										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	1	1	Configure Information
	W	0	0	0	0	0	0	0	0	
	W	0	EIS	EFIFO	POLL		FIFOTHR			
Execution	W	PRETRK								

RELATIVE SEEK										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	1	DIR	0	0	1	1	1	1	
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	RCN								

DUMPREG										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	1	1	0	*Note: Registers placed in FIFO
Execution										
Result	R	PCN-Drive 0								
	R	PCN-Drive 1								
	R	PCN-Drive 2								
	R	PCN-Drive 3								
	R	SRT						HUT		
	R	HLT							ND	
	R	SC/EOT								
	R	LOCK	0	D3	D2	D1	D0	GAP	WGATE	
	R	0	EIS	EFIFO	POLL		FIFOTHR			
	R	PRETRK								

READ ID										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	1	0	1	0	Commands
	W	0	0	0	0	0	HDS	DS1	DS0	
Execution										The first correct ID information on the Cylinder is stored in Data Register
Result	R					ST0				Status information after Command execution.
										Disk status after the Command has completed
	R					ST1				
	R					ST2				
	R					C				
	R					H				
	R					R				
	R					N				

PERPENDICULAR MODE										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	1	0	Command Codes
		OW	0	D3	D2	D1	D0	GAP	WGATE	

INVALID CODES										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	Invalid Codes								Invalid Command Codes (NoOp – FDC goes into Standby State)
Result	R	ST0								ST0 = 80H

LOCK										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	LOCK	0	0	1	0	1	0	0	Command Codes
Result	R	0	0	0	LOCK	0	0	0	0	

SC is returned if the last command that was issued was the Format command. EOT is returned if the last command was a Read or Write.

Note 8.11 These bits are used internally only. They are not reflected in the Drive Select pins. It is the user's responsibility to maintain correspondence between these bits and the Drive Select pins (DOR).

8.7.7 Data Transfer Commands

All of the Read Data, Write Data and Verify type commands use the same parameter bytes and return the same results information, the only difference being the coding of bits 0-4 in the first byte.

An implied seek will be executed if the feature was enabled by the Configure command. This seek is completely transparent to the user. The Drive Busy bit for the drive will go active in the Main Status Register during the seek portion of the command. If the seek portion fails, it is reflected in the results status normally returned for a Read/Write Data command. Status Register 0 (ST0) would contain the error code and C would contain the cylinder on which the seek failed.

8.7.7.1 Read Data

A set of nine (9) bytes is required to place the FDC in the Read Data Mode. After the Read Data command has been issued, the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify command), and begins reading ID Address Marks and ID fields. When the sector address read off the diskette matches with the sector address specified in the command, the FDC reads the sector's data field and transfers the data to the FIFO.

After completion of the read operation from the current sector, the sector address is incremented by one and the data from the next logical sector is read and output via the FIFO. This continuous read function is called "Multi-Sector Read Operation". Upon receipt of the TC cycle, or an implied TC (FIFO overrun/underrun), the FDC stops sending data but will continue to read data from the current sector, check the CRC bytes, and at the end of the sector, terminate the Read Data Command.

N determines the number of bytes per sector (see Table 8.23 below). If N is set to zero, the sector size is set to 128. The DTL value determines the number of bytes to be transferred. If DTL is less than 128, the FDC transfers the specified number of bytes to the host. For reads, it continues to read the entire 128-byte sector and checks for CRC errors. For writes, it completes the 128-byte sector by filling in zeros. If N is not set to 00 Hex, DTL should be set to FF Hex and has no impact on the number of bytes transferred.

Table 8.23 - Sector Sizes

N	SECTOR SIZE
00	128 bytes
01	256 bytes
02	512 bytes
03	1024 bytes
..	...
07	16 Kbytes

The amount of data which can be handled with a single command to the FDC depends upon MT (multi-track) and N (number of bytes/sector).

The Multi-Track function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 1, Side 0 and completing the last sector of the same track at Side 1.

If the host terminates a read or write operation in the FDC, the ID information in the result phase is dependent upon the state of the MT bit and EOT byte. Refer to Table 8.24.

At the completion of the Read Data command, the head is not unloaded until after the Head Unload Time Interval (specified in the Specify command) has elapsed. If the host issues another command before the head unloads, then the head settling time may be saved between subsequent reads.

If the FDC detects a pulse on the nINDEX pin twice without finding the specified sector (meaning that the diskette's index hole passes through index detect logic in the drive twice), the FDC sets the IC code in Status Register 0 to "01" indicating abnormal termination, sets the ND bit in Status Register 1 to "1" indicating a sector not found, and terminates the Read Data Command.

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If a CRC error occurs in the ID or data field, the FDC sets the IC code in Status Register 0 to "01" indicating abnormal termination, sets the DE bit flag in Status Register 1 to "1", sets the DD bit in Status Register 2 to "1" if CRC is incorrect in the ID field, and terminates the Read Data Command. Table 8.25 describes the effect of the SK bit on the Read Data command execution and results. Except where noted in Table 8.25, the C or R value of the sector address is automatically incremented (see Table 8.27).

Table 8.24 - Effects of MT and N Bits

MT	N	MAXIMUM TRANSFER CAPACITY	FINAL SECTOR READ FROM DISK
0	1	256 x 26 = 6,656	26 at side 0 or 1
1	1	256 x 52 = 13,312	26 at side 1
0	2	512 x 15 = 7,680	15 at side 0 or 1
1	2	512 x 30 = 15,360	15 at side 1
0	3	1024 x 8 = 8,192	8 at side 0 or 1
1	3	1024 x 16 = 16,384	16 at side 1

Table 8.25 - Skip Bit vs Read Data command

SK BIT VALUE	DATA ADDRESS MARK TYPE ENCOUNTERED	RESULTS		
		SECTOR READ?	CM BIT OF ST2 SET?	DESCRIPTION OF RESULTS
0	Normal Data	Yes	No	Normal termination.
0	Deleted Data	Yes	Yes	Address not incremented. Next sector not searched for.
1	Normal Data	Yes	No	Normal termination.
1	Deleted Data	No	Yes	Normal termination. Sector not read ("skipped").

8.7.7.2 Read Deleted Data

This command is the same as the Read Data command, only it operates on sectors that contain a Deleted Data Address Mark at the beginning of a Data Field.

Table 8.26 describes the effect of the SK bit on the Read Deleted Data command execution and results.

Except where noted in Table 8.26, the C or R value of the sector address is automatically incremented (see Table 8.27).

Table 8.26 - Skip Bit vs. Read Deleted Data Command

SK BIT VALUE	DATA ADDRESS MARK TYPE ENCOUNTERED	RESULTS		
		SECTOR READ?	CM BIT OF ST2 SET?	DESCRIPTION OF RESULTS
0	Normal Data	Yes	Yes	Address not incremented. Next sector not searched for.
0	Deleted Data	Yes	No	Normal termination.
1	Normal Data	No	Yes	Normal termination. Sector not read ("skipped").
1	Deleted Data	Yes	No	Normal termination.

8.7.7.3 Read A Track

This command is similar to the Read Data command except that the entire data field is read continuously from each of the sectors of a track. Immediately after encountering a pulse on the nINDEX pin, the FDC starts to read all data fields on the track as continuous blocks of data without regard to logical sector numbers. If the FDC finds an error in the ID or DATA CRC check bytes, it continues to read data from the track and sets the appropriate error bits at the end of the command. The FDC compares the ID information read from each sector with the specified value in the command and sets the ND flag of Status Register 1 to a “1” if there no comparison. Multi-track or skip operations are not allowed with this command. The MT and SK bits (bits D7 and D5 of the first command byte respectively) should always be set to "0".

This command terminates when the EOT specified number of sectors has not been read. If the FDC does not find an ID Address Mark on the diskette after the second occurrence of a pulse on the nINDEX pin, then it sets the IC code in Status Register 0 to "01" (abnormal termination), sets the MA bit in Status Register 1 to "1", and terminates the command.

Table 8.27 - Result Phase Table

MT	HEAD	FINAL SECTOR TRANSFERRED TO HOST	ID INFORMATION AT RESULT PHASE			
			C	H	R	N
0	0	Less than EOT	NC	NC	R + 1	NC
		Equal to EOT	C + 1	NC	01	NC
	1	Less than EOT	NC	NC	R + 1	NC
		Equal to EOT	C + 1	NC	01	NC
1	0	Less than EOT	NC	NC	R + 1	NC
		Equal to EOT	NC	LSB	01	NC
	1	Less than EOT	NC	NC	R + 1	NC
		Equal to EOT	C + 1	LSB	01	NC

NC: No Change, the same value as the one at the beginning of command execution.

LSB: Least Significant Bit, the LSB of H is complemented.

8.7.7.4 Write Data

After the Write Data command has been issued, the FDC loads the head (if it is in the unloaded state), waits the specified head load time if unloaded (defined in the Specify command), and begins reading ID fields. When the sector address read from the diskette matches the sector address specified in the command, the FDC reads the data from the host via the FIFO and writes it to the sector's data field.

After writing data into the current sector, the FDC computes the CRC value and writes it into the CRC field at the end of the sector transfer. The Sector Number stored in "R" is incremented by one, and the FDC continues writing to the next data field. The FDC continues this "Multi-Sector Write Operation". Upon receipt of a terminal count signal or if a FIFO over/under run occurs while a data field is being written, then the remainder of the data field is filled with zeros. The FDC reads the ID field of each sector and checks the CRC bytes. If it detects a CRC error in one of the ID fields, it sets the IC code in Status Register 0 to "01" (abnormal termination), sets the DE bit of Status Register 1 to "1", and terminates the Write Data command.

The Write Data command operates in much the same manner as the Read Data command. The following items are the same. Please refer to the Read Data Command for details:

- Transfer Capacity
- EN (End of Cylinder) bit
- ND (No Data) bit
- Head Load, Unload Time Interval
- ID information when the host terminates the command
- Definition of DTL when N = 0 and when N does not = 0

8.7.7.5 Write Deleted Data

This command is almost the same as the Write Data command except that a Deleted Data Address Mark is written at the beginning of the Data Field instead of the normal Data Address Mark. This command is typically used to mark a bad sector containing an error on the floppy disk.

8.7.7.6 Verify

The Verify command is used to verify the data stored on a disk. This command acts exactly like a Read Data command except that no data is transferred to the host. Data is read from the disk and CRC is computed and checked against the previously-stored value.

Because data is not transferred to the host, the TC cycle cannot be used to terminate this command. By setting the EC bit to "1", an implicit TC will be issued to the FDC. This implicit TC will occur when the SC value has decremented to 0 (an SC value of 0 will verify 256 sectors). This command can also be terminated by setting the EC bit to "0" and the EOT value equal to the final sector to be checked. If EC is set to "0", DTL/SC should be programmed to 0FFH. Refer to Table 8.27 and Table 8.28 for information concerning the values of MT and EC versus SC and EOT value.

Definitions:

Sectors Per Side = Number of formatted sectors per each side of the disk.

Sectors Remaining = Number of formatted sectors left which can be read, including side 1 of the disk if MT is set to "1".

Table 8.28 - Verify Command Result Phase Table

MT	EC	SC/EOT VALUE	TERMINATION RESULT
0	0	SC = DTL EOT <= # Sectors Per Side	Success Termination Result Phase Valid
0	0	SC = DTL EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid
0	1	SC <= # Sectors Remaining AND EOT <= # Sectors Per Side	Successful Termination Result Phase Valid
0	1	SC > # Sectors Remaining OR EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid
1	0	SC = DTL EOT <= # Sectors Per Side	Successful Termination Result Phase Valid
1	0	SC = DTL EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid
1	1	SC <= # Sectors Remaining AND EOT <= # Sectors Per Side	Successful Termination Result Phase Valid
1	1	SC > # Sectors Remaining OR EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid

Note 8.12 If MT is set to "1" and the SC value is greater than the number of remaining formatted sectors on Side 0, verifying will continue on Side 1 of the disk.

8.7.7.7 Format A Track

The Format command allows an entire track to be formatted. After a pulse from the nINDEX pin is detected, the FDC starts writing data on the disk including gaps, address marks, ID fields, and data fields per the IBM System 34 or 3740 format (MFM or FM respectively). The particular values that will be written to the gap and data field are controlled by the values programmed into N, SC, GPL, and D which are specified by the host during the command phase. The data field of the sector is filled with the data byte specified by D. The ID field for each sector is supplied by the host; that is, four data bytes per sector are needed by the FDC for C, H, R, and N (cylinder, head, sector number and sector size respectively).

After formatting each sector, the host must send new values for C, H, R and N to the FDC for the next sector on the track. The R value (sector number) is the only value that must be changed by the host after each sector is formatted. This allows the disk to be formatted with nonsequential sector addresses (interleaving). This incrementing and formatting continues for the whole track until the FDC encounters a pulse on the nINDEX pin again and it terminates the command.

Table 8.29 contains typical values for gap fields which are dependent upon the size of the sector and the number of sectors on each track. Actual values can vary due to drive electronics.

FORMAT FIELDS

SYSTEM 34 (DOUBLE DENSITY) FORMAT

GAP4a 80x 4E	SYNC 12x 00	IAM		GAP1 50x 4E	SYNC 12x 00	IDAM		CYL	HD	SEC	NO	CRC	GAP2 22x 4E	SYNC 12x 00	DATA AM		DATA	CRC	GAP3	GAP 4b
		3x C2	FC			3x A1	FE								3x A1	FB F8				

SYSTEM 3740 (SINGLE DENSITY) FORMAT

GAP4a 40x FF	SYNC 6x 00	IAM	GAP1 26x FF	SYNC 6x 00	IDAM	CYL	HD	SEC	NO	CRC	GAP2 11x FF	SYNC 6x 00	DATA AM	DATA	CRC	GAP3	GAP 4b
		FC			FE								FB or F8				

PERPENDICULAR FORMAT

GAP4a 80x 4E	SYNC 12x 00	IAM		GAP1 50x 4E	SYNC 12x 00	IDAM		CYL	HD	SEC	NO	CRC	GAP2 41x 4E	SYNC 12x 00	DATA AM		DATA	CRC	GAP3	GAP 4b
		3x C2	FC			3x A1	FE								3x A1	FB F8				

Table 8.29 - Typical Values for Formatting

	FORMAT	SECTOR SIZE	N	SC	GPL1	GPL2
5.25" Drives	FM	128	00	12	07	09
		128	00	10	10	19
		512	02	08	18	30
		1024	03	04	46	87
		2048	04	02	C8	FF
		4096	05	01	C8	FF
		...	...			
	MFM	256	01	12	0A	0C
		256	01	10	20	32
		512*	02	09	2A	50
		1024	03	04	80	F0
		2048	04	02	C8	FF
		4096	05	01	C8	FF
		...	...			
3.5" Drives	FM	128	0	0F	07	1B
		256	1	09	0F	2A
		512	2	05	1B	3A
	MFM	256	1	0F	0E	36
		512**	2	09	1B	54
		1024	3	05	35	74

GPL1 = suggested GPL values in Read and Write commands to avoid splice point between data field and ID field of contiguous sections.

GPL2 = suggested GPL value in Format A Track command.

*PC/AT values (typical)

**PS/2 values (typical). Applies with 1.0 MB and 2.0 MB drives.

Note 8.13 All values except sector size are in hex.

8.7.8 Control Commands

Control commands differ from the other commands in that no data transfer takes place. Three commands generate an interrupt when complete: Read ID, Recalibrate, and Seek. The other control commands do not generate an interrupt.

8.7.8.1 Read ID

The Read ID command is used to find the present position of the recording heads. The FDC stores the values from the first ID field it is able to read into its registers. If the FDC does not find an ID address mark on the diskette after the second occurrence of a pulse on the nINDEX pin, it then sets the IC code in Status Register 0 to "01" (abnormal termination), sets the MA bit in Status Register 1 to "1", and terminates the command.

The following commands will generate an interrupt upon completion. They do not return any result bytes. It is highly recommended that control commands be followed by the Sense Interrupt Status command. Otherwise, valuable interrupt status information will be lost.

8.7.8.2 Recalibrate

This command causes the read/write head within the FDC to retract to the track 0 position. The FDC clears the contents of the PCN counter and checks the status of the nTRK0 pin from the FDD. As long as the nTRK0 pin is low, the DIR pin remains 0 and step pulses are issued. When the nTRK0 pin goes high, the SE bit in Status Register 0 is set to "1" and the command is terminated. If the nTR0 pin is still low after 255 step pulses have been issued, the FDC sets the SE and the EC bits of Status Register 0 to "1" and terminates the command. Disks capable of handling more than 255 tracks per side may require more than one Recalibrate command to return the head back to physical Track 0.

The Recalibrate command does not have a result phase. The Sense Interrupt Status command must be issued after the Recalibrate command to effectively terminate it and to provide verification of the head position (PCN). During the command phase of the recalibrate operation, the FDC is in the BUSY state, but during the execution phase it is in a NON-BUSY state. At this time, another Recalibrate command may be issued, and in this manner parallel Recalibrate operations may be done on up to four drives at once. Upon power up, the software must issue a Recalibrate command to properly initialize all drives and the controller.

8.7.8.3 Seek

The read/write head within the drive is moved from track to track under the control of the Seek command. The FDC compares the PCN, which is the current head position, with the NCN and performs the following operation if there is a difference:

PCN < NCN: Direction signal to drive set to "1" (step in) and issues step pulses.

PCN > NCN: Direction signal to drive set to "0" (step out) and issues step pulses.

The rate at which step pulses are issued is controlled by SRT (Stepping Rate Time) in the Specify command. After each step pulse is issued, NCN is compared against PCN, and when NCN = PCN the SE bit in Status Register 0 is set to "1" and the command is terminated. During the command phase of the seek or recalibrate operation, the FDC is in the BUSY state, but during the execution phase it is in the NON-BUSY state. At this time, another Seek or Recalibrate command may be issued, and in this manner, parallel seek operations may be done on up to four drives at once.

NOTE: If implied seek is not enabled, the read and write commands should be preceded by:

1) Seek command - Step to the proper track

2) Sense Interrupt Status command - Terminate the Seek command

3) Read ID - Verify head is on proper track

4) Issue Read/Write command.

The Seek command does not have a result phase. Therefore, it is highly recommended that the Sense Interrupt Status command is issued after the Seek command to terminate it and to provide verification of the head position (PCN). The H bit (Head Address) in ST0 will always return to a "0". When exiting POWERDOWN mode, the FDC clears the PCN value and the status information to zero. Prior to issuing the POWERDOWN command, it is highly recommended that the user service all pending interrupts through the Sense Interrupt Status command.

8.7.8.4 Sense Interrupt Status

An interrupt signal is generated by the FDC for one of the following reasons:

1) Upon entering the Result Phase of:
    1) Read Data command
    2) Read A Track command
    3) Read ID command
    4) Read Deleted Data command
    5) Write Data command
    6) Format A Track command
    7) Write Deleted Data command
    8) Verify command
2) End of Seek, Relative Seek, or Recalibrate command

The Sense Interrupt Status command resets the interrupt signal and, via the IC code and SE bit of Status Register 0, identifies the cause of the interrupt.

Table 8.30 - Interrupt Identification

SE	IC	INTERRUPT DUE TO
0	11	Polling
1	00	Normal termination of Seek or Recalibrate command
1	01	Abnormal termination of Seek or Recalibrate command

The Seek, Relative Seek, and Recalibrate commands have no result phase. The Sense Interrupt Status command must be issued immediately after these commands to terminate them and to provide verification of the head position (PCN). The H (Head Address) bit in ST0 will always return a "0". If a Sense Interrupt Status is not issued, the drive will continue to be BUSY and may affect the operation of the next command.

8.7.8.5 Sense Drive Status

Sense Drive Status obtains drive status information. It has not execution phase and goes directly to the result phase from the command phase. Status Register 3 contains the drive status information.

8.7.8.6 Specify

The Specify command sets the initial values for each of the three internal times. The HUT (Head Unload Time) defines the time from the end of the execution phase of one of the read/write commands to the head unload state. The SRT (Step Rate Time) defines the time interval between adjacent step pulses. Note that the spacing between the first and second step pulses may be shorter than the remaining step pulses. The HLT (Head Load Time) defines the time between when the Head Load signal goes high and the read/write operation starts. The values change with the data rate speed selection and are documented in Table 8.31. The values are the same for MFM and FM.

DMA operation is selected by the ND bit. When ND is "0", the DMA mode is selected. In DMA mode, data transfers are signaled by the DMA request cycles.

8.7.8.7 Configure

The Configure command is issued to select the special features of the FDC. A Configure command need not be issued if the default values of the FDC meet the system requirements.

Table 8.31 - Drive Control Delays (ms)

	HUT					SRT				
	2M	**1M**	**500K**	**300K**	**250K**	**2M**	**1M**	**500K**	**300K**	**250K**
0	64	128	256	426	512	4	8	16	26.7	32
1	4	8	16	26.7	32	3.75	7.5	15	25	30
..	..	..	..	..	..	..	..	..	..	..
E	56	112	224	373	448	0.5	1	2	3.33	4
F	60	120	240	400	480	0.25	0.5	1	1.67	2

	HLT				
	2M	**1M**	**500K**	**300K**	**250K**
00	64	128	256	426	512
01	0.5	1	2	3.3	4
02	1	2	4	6.7	8
..	..	..	..	..	.
7F	63	126	252	420	504
7F	63.5	127	254	423	508

Configure Default Values:

- EIS - No Implied Seeks
- EFIFO - FIFO Disabled
- POLL - Polling Enabled
- FIFOTHR - FIFO Threshold Set to 1 Byte
- PRETRK - Pre-Compensation Set to Track 0

EIS - Enable Implied Seek. When set to "1", the FDC will perform a Seek operation before executing a read or write command. Defaults to no implied seek.

EFIFO - A "1" disables the FIFO (default). This means data transfers are asked for on a byte-by-byte basis. Defaults to "1", FIFO disabled. The threshold defaults to "1".

POLL - Disable polling of the drives. Defaults to "0", polling enabled. When enabled, a single interrupt is generated after a reset. No polling is performed while the drive head is loaded and the head unload delay has not expired.

FIFOTHR - The FIFO threshold in the execution phase of read or write commands. This is programmable from 1 to 16 bytes. Defaults to one byte. A "00" selects one byte; "0F" selects 16 bytes.

PRETRK - Pre-Compensation Start Track Number. Programmable from track 0 to 255. Defaults to track 0. A "00" selects track 0; "FF" selects track 255.

8.7.8.8 Version

The Version command checks to see if the controller is an enhanced type or the older type (765A). A value of 90 H is returned as the result byte.

8.7.8.9 Relative Seek

The command is coded the same as for Seek, except for the MSB of the first byte and the DIR bit.

- DIR Head Step Direction Control
- RCN Relative Cylinder Number that determines how many tracks to step the head in or out from the current track number.

DIR	ACTION
0	Step Head Out
1	Step Head In

The Relative Seek command differs from the Seek command in that it steps the head the absolute number of tracks specified in the command instead of making a comparison against an internal register. The Seek command is good for drives that support a maximum of 256 tracks. Relative Seeks cannot be overlapped with other Relative Seeks. Only one Relative Seek can be active at a time. Relative Seeks may be overlapped with Seeks and Recalibrates. Bit 4 of Status Register 0 (EC) will be set if Relative Seek attempts to step outward beyond Track 0.

As an example, assume that a floppy drive has 300 useable tracks. The host needs to read track 300 and the head is on any track (0-255). If a Seek command is issued, the head will stop at track 255. If a Relative Seek command is issued, the FDC will move the head the specified number of tracks, regardless of the internal cylinder position register (but will increment the register). If the head was on track 40 (d), the maximum track that the FDC could position the head on using Relative Seek will be 295 (D), the initial track + 255 (D). The maximum count that the head can be moved with a single Relative Seek command is 255 (D).

The internal register, PCN, will overflow as the cylinder number crosses track 255 and will contain 39 (D). The resulting PCN value is thus (RCN + PCN) mod 256. Functionally, the FDC starts counting from 0 again as the track number goes above 255 (D). It is the user's responsibility to compensate FDC functions (precompensation track number) when accessing tracks greater than 255. The FDC does not keep track that it is working in an "extended track area" (greater than 255). Any command issued will use the current PCN value except for the Recalibrate command, which only looks for the TRACK0 signal. Recalibrate will return an error if the head is farther than 255 due to its limitation of issuing a maximum of 255 step pulses. The user simply needs to issue a second Recalibrate command. The Seek command and implied seeks will function correctly within the 44 (D) track (299-255) area of the "extended track area". It is the user's responsibility not to issue a new track position that will exceed the maximum track that is present in the extended area.

To return to the standard floppy range (0-255) of tracks, a Relative Seek should be issued to cross the track 255 boundary.

A Relative Seek can be used instead of the normal Seek, but the host is required to calculate the difference between the current head location and the new (target) head location. This may require the host to issue a Read ID command to ensure that the head is physically on the track that software assumes it to be. Different FDC commands will return different cylinder results which may be difficult to keep track of with software without the Read ID command.

8.7.8.10 Perpendicular Mode

The Perpendicular Mode command should be issued prior to executing Read/Write/Format commands that access a disk drive with perpendicular recording capability. With this command, the length of the Gap2 field and VCO enable timing can be altered to accommodate the unique requirements of these drives. Table 8.32 describes the effects of the WGATE and GAP bits for the Perpendicular Mode command. Upon a reset, the FDC will default to the conventional mode (WGATE = 0, GAP = 0).

Selection of the 500 Kbps and 1 Mbps perpendicular modes is independent of the actual data rate selected in the Data Rate Select Register. The user must ensure that these two data rates remain consistent.

The Gap2 and VCO timing requirements for perpendicular recording type drives are dictated by the design of the read/write head. In the design of this head, a pre-erase head precedes the normal read/write head by a distance of 200 micrometers. This works out to about 38 bytes at a 1 Mbps recording density. Whenever the write head is enabled by the Write Gate signal, the pre-erase head is also activated at the same time. Thus, when the write head is initially turned on, flux transitions recorded on the media for the first 38 bytes will not be preconditioned with the pre-erase head since it has not yet been activated. To accommodate this head activation and deactivation time, the Gap2 field is expanded to a length of 41 bytes. The Format Fields table illustrates the change in the Gap2 field size for the perpendicular format.

On the read back by the FDC, the controller must begin synchronization at the beginning of the sync field. For the conventional mode, the internal PLL VCO is enabled (VCOEN) approximately 24 bytes from the start of the Gap2 field. But, when the controller operates in the 1 Mbps perpendicular mode (WGATE = 1, GAP = 1), VCOEN goes active after 43 bytes to accommodate the increased Gap2 field size. For both cases, and approximate two-byte cushion is maintained from the beginning of the sync field for the purposes of avoiding write splices in the presence of motor speed variation.

For the Write Data case, the FDC activates Write Gate at the beginning of the sync field under the conventional mode. The controller then writes a new sync field, data address mark, data field, and CRC. With the pre-erase head of the perpendicular drive, the write head must be activated in the Gap2 field to insure a proper write of the new sync field. For the 1 Mbps perpendicular mode (WGATE = 1, GAP = 1), 38 bytes will be written in the Gap2 space. Since the bit density is proportional to the data rate, 19 bytes will be written in the Gap2 field for the 500 Kbps perpendicular mode (WGATE = 1, GAP =0).

It should be noted that none of the alterations in Gap2 size, VCO timing, or Write Gate timing affect normal program flow. The information provided here is just for background purposes and is not needed for normal operation. Once the Perpendicular Mode command is invoked, FDC software behavior from the user standpoint is unchanged.

The perpendicular mode command is enhanced to allow specific drives to be designated Perpendicular recording drives. This enhancement allows data transfers between Conventional and Perpendicular drives without having to issue Perpendicular mode commands between the accesses of the different drive types, nor having to change write pre-compensation values.

When both GAP and WGATE bits of the PERPENDICULAR MODE COMMAND are both programmed to "0" (Conventional mode), then D0, D1, D2, D3, and D4 can be programmed independently to "1" for that drive to be set automatically to Perpendicular mode. In this mode the following set of conditions also apply:

1) The GAP2 written to a perpendicular drive during a write operation will depend upon the programmed data rate.

2) The write pre-compensation given to a perpendicular mode drive will be 0ns.

3) For D0-D3 programmed to "0" for conventional mode drives any data written will be at the currently programmed write pre-compensation.

NOTE: Bits D0-D3 can only be overwritten when OW is programmed as a "1". If either GAP or WGATE is a "1" then D0-D3 are ignored.

Software and hardware resets have the following effect on the PERPENDICULAR MODE COMMAND:

1) "Software" resets (via the DOR or DSR registers) will only clear GAP and WGATE bits to "0". D0-D3 are unaffected and retain their previous value.

2) "Hardware" resets will clear all bits (GAP, WGATE and D0-D3) to "0", i.e all conventional mode.

Table 8.32 - Effects of WGATE and GAP Bits

WGATE	GAP	MODE	LENGTH OF GAP2 FORMAT FIELD	PORTION OF GAP 2 WRITTEN BY WRITE DATA OPERATION
0	0	Conventional	22 Bytes	0 Bytes
0	1	Perpendicular (500 Kbps)	22 Bytes	19 Bytes
1	0	Reserved (Conventional)	22 Bytes	0 Bytes
1	1	Perpendicular (1 Mbps)	41 Bytes	38 Bytes

8.7.8.11 Lock

In order to protect systems with long DMA latencies against older application software that can disable the FIFO the LOCK Command has been added. This command should only be used by the FDC routines, and application software should refrain from using it. If an application calls for the FIFO to be disabled then the CONFIGURE command should be used.

The LOCK command defines whether the EFIFO, FIFOTHR, and PRETRK parameters of the CONFIGURE command can be RESET by the DOR and DSR registers. When the LOCK bit is set to logic "1" all subsequent "software RESETS by the DOR and DSR registers will not change the previously set parameters to their default values. All "hardware" RESET from the PCI_RESET# pin will set the LOCK bit to logic "0" and return the EFIFO, FIFOTHR, and PRETRK to their default values. A status byte is returned immediately after issuing a LOCK command. This byte reflects the value of the LOCK bit set by the command byte.

8.7.8.12 Enhanced DUMPREG

The DUMPREG command is designed to support system run-time diagnostics and application software development and debug. To accommodate the LOCK command and the enhanced PERPENDICULAR MODE command the eighth byte of the DUMPREG command has been modified to contain the additional data from these two commands.

8.7.8.13 Compatibility

The SIO10N268 was designed with software compatibility in mind. It is a fully backwards- compatible solution with the older generation 765A/B disk controllers. The FDC also implements on-board registers for compatibility with the PS/2, as well as PC/AT and PC/XT, floppy disk controller subsystems. After a hardware reset of the FDC, all registers, functions and enhancements default to a PC/AT, PS/2 or PS/2 Model 30 compatible operating mode, depending on how the IDENT and MFM bits are configured by the system BIOS.

8.8 Serial Port (UART)

The SIO10N268 incorporates four full function UARTs. They are compatible with the 16450, the 16450 ACE registers and the 16C550A. The UARTS perform serial-to-parallel conversion on received characters and parallel-to-serial conversion on transmit characters. The data rates are independently programmable from 460.8K baud down to 50 baud. The character options are programmable for 1 start; 1, 1.5 or 2 stop bits; even, odd, sticky or no parity; and prioritized interrupts. The UARTs each contain a programmable baud rate generator that is capable of dividing the input clock or crystal by a number from 1 to 65535. The UARTs are also capable of supporting the MIDI data rate. Refer to the Configuration Registers for information on disabling, power down and changing the base address of the UARTs. The interrupt from a UART is enabled by programming OUT2 of that UART to a logic "1". OUT2 being a logic "0" disables that UART's interrupt. The second UART also supports IrDA 1.2 (4Mbps), HP-SIR, ASK-IR and Consumer IR infrared modes of operation.

8.8.1 Register Description

Addressing of the accessible registers of the Serial Port is shown below. The base addresses of the serial ports are defined by the configuration registers (see Configuration section). The Serial Port registers are located at sequentially increasing addresses above these base addresses. The SIO10N268 contains two serial ports, each of which contain a register set as described below.

Table 8.33 - Addressing the Serial Port

DLAB*	A2	A1	A0	REGISTER NAME
0	0	0	0	Receive Buffer (read)
0	0	0	0	Transmit Buffer (write)
0	0	0	1	Interrupt Enable (read/write)
X	0	1	0	Interrupt Identification (read)
X	0	1	0	FIFO Control (write)
X	0	1	1	Line Control (read/write)
X	1	0	0	Modem Control (read/write)
X	1	0	1	Line Status (read/write)
X	1	1	0	Modem Status (read/write)
X	1	1	1	Scratchpad (read/write)
1	0	0	0	Divisor LSB (read/write)
1	0	0	1	Divisor MSB (read/write

Note 8.14 DLAB is Bit 7 of the Line Control Register

The following section describes the operation of the registers.

8.8.1.1 Receive Buffer Register (RB)

Address Offset = 0H, DLAB = 0, READ ONLY

This register holds the received incoming data byte. Bit 0 is the least significant bit, which is transmitted and received first. Received data is double buffered; this uses an additional shift register to receive the serial data stream and convert it to a parallel 8 bit word which is transferred to the Receive Buffer register. The shift register is not accessible.

8.8.1.2 Transmit Buffer Register (TB)

Address Offset = 0H, DLAB = 0, WRITE ONLY

This register contains the data byte to be transmitted. The transmit buffer is double buffered, utilizing an additional shift register (not accessible) to convert the 8 bit data word to a serial format. This shift register is loaded from the Transmit Buffer when the transmission of the previous byte is complete.

8.8.1.3 Interrupt Enable Register (IER)

Address Offset = 1H, DLAB = 0, READ/WRITE

The lower four bits of this register control the enables of the five interrupt sources of the Serial Port interrupt. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of this register. Similarly, setting the appropriate bits of this register to a high, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and disables any Serial Port interrupt out of the SIO10N268. All other system functions operate in their normal manner, including the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are described below.

Bit 0

This bit enables the Received Data Available Interrupt (and timeout interrupts in the FIFO mode) when set to logic "1".

Bit 1

This bit enables the Transmitter Holding Register Empty Interrupt when set to logic "1".

Bit 2

This bit enables the Received Line Status Interrupt when set to logic "1". The error sources causing the interrupt are Overrun, Parity, Framing and Break. The Line Status Register must be read to determine the source.

Bit 3

This bit enables the MODEM Status Interrupt when set to logic "1". This is caused when one of the Modem Status Register bits changes state.

Bits 4 through 7

These bits are always logic "0".

8.8.1.4 FIFO Control Register (FCR)

Address Offset = 2H, DLAB = X, WRITE

This is a write only register at the same location as the IIR. This register is used to enable and clear the FIFOs, set the RCVR FIFO trigger level. Note: DMA is not supported. The UART1 and UART2 FCR's are shadowed in the UART1 FIFO Control Shadow Register (CR15) and UART2 FIFO Control Shadow Register (CR16). See the Configuration section for description on these registers.

Bit 0

Setting this bit to a logic "1" enables both the XMIT and RCVR FIFOs. Clearing this bit to a logic "0" disables both the XMIT and RCVR FIFOs and clears all bytes from both FIFOs. When changing from FIFO Mode to non-FIFO (16450) mode, data is automatically cleared from the FIFOs. This bit must be a 1 when other bits in this register are written to or they will not be properly programmed.

Bit 1

Setting this bit to a logic "1" clears all bytes in the RCVR FIFO and resets its counter logic to 0. The shift register is not cleared. This bit is self-clearing.

Bit 2

Setting this bit to a logic "1" clears all bytes in the XMIT FIFO and resets its counter logic to 0. The shift register is not cleared. This bit is self-clearing.

Bit 3

Writing to this bit has no effect on the operation of the UART. DMA modes are not supported in this chip.

Bit 4,5

Reserved

Bit 6,7

These bits are used to set the trigger level for the RCVR FIFO interrupt.

Bit 7	Bit 6	RCVR FIFO Trigger Level (BYTES)
0	0	1
0	1	4
1	0	8
1	1	14

8.8.1.5 Interrupt Identification Register (IIR)

Address Offset = 2H, DLAB = X, READ

By accessing this register, the host CPU can determine the highest priority interrupt and its source. Four levels of priority interrupt exist. They are in descending order of priority:

1) Receiver Line Status (highest priority)

2) Received Data Ready

3) Transmitter Holding Register Empty

4) MODEM Status (lowest priority)

Information indicating that a prioritized interrupt is pending and the source of that interrupt is stored in the Interrupt Identification Register (refer to Interrupt Control Table). When the CPU accesses the IIR, the Serial Port freezes all interrupts and indicates the highest priority pending interrupt to the CPU. During this CPU access, even if the Serial Port records new interrupts, the current indication does not change until access is completed. The contents of the IIR are described below.

Bit 0

This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic "0", an interrupt is pending and the contents of the IIR may be used as a pointer to the appropriate internal service routine. When bit 0 is a logic "1", no interrupt is pending.

Bits 1 and 2

These two bits of the IIR are used to identify the highest priority interrupt pending as indicated by the Interrupt Control Table.

Bit 3

In non-FIFO mode, this bit is a logic "0". In FIFO mode this bit is set along with bit 2 when a timeout interrupt is pending.

Bits 4 and 5

These bits of the IIR are always logic "0".

Bits 6 and 7

These two bits are set when the FIFO CONTROL Register bit 0 equals 1.

Table 8.34 - Interrupt Control Table

FIFO MODE ONLY	INTERRUPT IDENTIFICATION REGISTER			INTERRUPT SET AND RESET FUNCTIONS			
BIT 3	BIT 2	BIT 1	BIT 0	PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET CONTROL
0	0	0	1	-	None	None	-
0	1	1	0	Highest	Receiver Line Status	Overrun Error, Parity Error, Framing Error or Break Interrupt	Reading the Line Status Register
0	1	0	0	Second	Received Data Available	Receiver Data Available	Read Receiver Buffer or the FIFO drops below the trigger level.
1	1	0	0	Second	Character	No Characters	Reading the

FIFO MODE ONLY	INTERRUPT IDENTIFICATION REGISTER			INTERRUPT SET AND RESET FUNCTIONS			
BIT 3	BIT 2	BIT 1	BIT 0	PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET CONTROL
					Timeout Indication	Have Been Removed From or Input to the RCVR FIFO during the last 4 Char times and there is at least 1 char in it during this time	Receiver Buffer Register
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if Source of Interrupt) or Writing the Transmitter Holding Register
0	0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect	Reading the MODEM Status Register

8.8.1.6 Line Control Register (LCR)

Address Offset = 3H, DLAB = 0, READ/WRITE

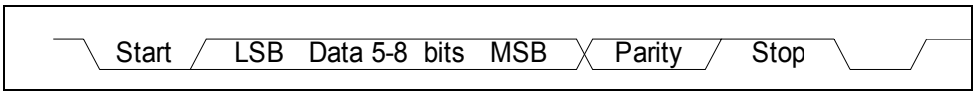


Figure 8.7 - Serial Data

This register contains the format information of the serial line. The bit definitions are:

Bits 0 and 1

These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

The Start, Stop and Parity bits are not included in the word length.

BIT 1	BIT 0	WORD LENGTH
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2

This bit specifies the number of stop bits in each transmitted or received serial character. The following table summarizes the information.

BIT 2	WORD LENGTH	NUMBER OF STOP BITS
0	--	1
1	5 bits	1.5
1	6 bits	2
1	7 bits	2
1	8 bits	2

NOTE: The receiver will ignore all stop bits beyond the first, regardless of the number used in transmitting.

Bit 3

Parity Enable bit. When bit 3 is a logic "1", a parity bit is generated (transmit data) or checked (receive data) between the last data word bit and the first stop bit of the serial data. (The parity bit is used to generate an even or odd number of 1s when the data word bits and the parity bit are summed).

Bit 4

Even Parity Select bit. When bit 3 is a logic "1" and bit 4 is a logic "0", an odd number of logic "1"'s is transmitted or checked in the data word bits and the parity bit. When bit 3 is a logic "1" and bit 4 is a logic "1" an even number of bits is transmitted and checked.

Bit 5

Stick Parity bit. When parity is enabled it is used in conjunction with bit 4 to select Mark or Space Parity. When LCR bits 3, 4 and 5 are 1 the Parity bit is transmitted and checked as 0 (Space Parity). If bits 3 and 5 are 1 and bit 4 is a 0, then the Parity bit is transmitted and checked as 1 (Mark Parity). If bit 5 is 0 Stick Parity is disabled.

Bit 6

Set Break Control bit. When bit 6 is a logic "1", the transmit data output (TXD) is forced to the Spacing or logic "0" state and remains there (until reset by a low level bit 6) regardless of other transmitter activity. This feature enables the Serial Port to alert a terminal in a communications system.

Bit 7

Divisor Latch Access bit (DLAB). It must be set high (logic "1") to access the Divisor Latches of the Baud Rate Generator during read or write operations. It must be set low (logic "0") to access the Receiver Buffer Register, the Transmitter Holding Register, or the Interrupt Enable Register.

8.8.1.7 Modem Control Register (MCR)

Address Offset = 4H, DLAB = X, READ/WRITE

This 8 bit register controls the interface with the MODEM or data set (or device emulating a MODEM). The contents of the MODEM control register are described below.

Bit 0

This bit controls the Data Terminal Ready (nDTR) output. When bit 0 is set to a logic "1", the nDTR output is forced to a logic "0". When bit 0 is a logic "0", the nDTR output is forced to a logic "1".

Bit 1

This bit controls the Request To Send (nRTS) output. Bit 1 affects the nRTS output in a manner identical to that described above for bit 0.

Bit 2

This bit controls the Output 1 (OUT1) bit. This bit does not have an output pin and can only be read or written by the CPU.

Bit 3

Output 2 (OUT2). This bit is used to enable an UART interrupt. When OUT2 is a logic "0", the serial port interrupt output is forced to a high impedance state - disabled. When OUT2 is a logic "1", the serial port interrupt outputs are enabled.

Bit 4

This bit provides the loopback feature for diagnostic testing of the Serial Port. When bit 4 is set to logic "1", the following occur:

1) The TXD is set to the Marking State(logic "1").
2) The receiver Serial Input (RXD) is disconnected.
3) The output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input.
4) All MODEM Control inputs (nCTS, nDSR, nRI and nDCD) are disconnected.
5) The four MODEM Control outputs (nDTR, nRTS, OUT1 and OUT2) are internally connected to the four MODEM Control inputs (nDSR, nCTS, RI, DCD).
6) The Modem Control output pins are forced inactive high.
7) Data that is transmitted is immediately received.

This feature allows the processor to verify the transmit and receive data paths of the Serial Port. In the diagnostic mode, the receiver and the transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

Bits 5 through 7

These bits are permanently set to logic zero.

8.8.1.8 Line Status Register (LSR)

Address Offset = 5H, DLAB = X, READ/WRITE

Bit 0

Data Ready (DR). It is set to a logic "1" whenever a complete incoming character has been received and transferred into the Receiver Buffer Register or the FIFO. Bit 0 is reset to a logic "0" by reading all of the data in the Receive Buffer Register or the FIFO.

Bit 1

Overrun Error (OE). Bit 1 indicates that data in the Receiver Buffer Register was not read before the next character was transferred into the register, thereby destroying the previous character. In FIFO mode, an overrunn error will occur only when the FIFO is full and the next character has been completely received in the shift register, the character in the shift register is overwritten but not transferred to the FIFO. The OE indicator is set to a logic "1" immediately upon detection of an overrun condition, and reset whenever the Line Status Register is read.

Bit 2

Parity Error (PE). Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even parity select bit. The PE is set to a logic "1" upon detection of a parity error and is reset to a logic "0" whenever the Line Status Register is read. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO.

Bit 3

Framing Error (FE). Bit 3 indicates that the received character did not have a valid stop bit. Bit 3 is set to a logic "1" whenever the stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level). The FE is reset to a logic "0" whenever the Line Status Register is read. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO. The Serial Port will try to resynchronize after a framing error. To do this, it assumes that the framing error was due to the next start bit, so it samples this 'start' bit twice and then takes in the 'data'.

Bit 4

Break Interrupt (BI). Bit 4 is set to a logic "1" whenever the received data input is held in the Spacing state (logic "0") for longer than a full word transmission time (that is, the total time of the start bit + data bits + parity bits + stop bits). The BI is reset after the CPU reads the contents of the Line Status Register. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO. When break occurs only one zero character is loaded into the FIFO. Restarting after a break is received, requires the serial data (RXD) to be logic "1" for at least 1/2 bit time.

NOTE: Bits 1 through 4 are the error conditions that produce a Receiver Line Status Interrupt whenever any of the corresponding conditions are detected and the interrupt is enabled.

Bit 5

Transmitter Holding Register Empty (THRE). Bit 5 indicates that the Serial Port is ready to accept a new character for transmission. In addition, this bit causes the Serial Port to issue an interrupt when the Transmitter Holding Register interrupt enable is set high. The THRE bit is set to a logic "1" when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic "0" whenever the CPU loads the Transmitter Holding Register. In the FIFO mode this bit is set when the XMIT FIFO is empty, it is cleared when at least 1 byte is written to the XMIT FIFO. Bit 5 is a read only bit.

Bit 6

Transmitter Empty (TEMT). Bit 6 is set to a logic "1" whenever the Transmitter Holding Register (THR) and Transmitter Shift Register (TSR) are both empty. It is reset to logic "0" whenever either the THR or

TSR contains a data character. Bit 6 is a read only bit. In the FIFO mode this bit is set whenever the THR and TSR are both empty.

Bit 7

This bit is permanently set to logic "0" in the 450 mode. In the FIFO mode, this bit is set to a logic "1" when there is at least one parity error, framing error or break indication in the FIFO. This bit is cleared when the LSR is read if there are no subsequent errors in the FIFO.

8.8.1.9 Modem Status Register (MSR)

Address Offset = 6H, DLAB = X, READ/WRITE

This 8 bit register provides the current state of the control lines from the MODEM (or peripheral device). In addition to this current state information, four bits of the MODEM Status Register (MSR) provide change information. These bits are set to logic "1" whenever a control input from the MODEM changes state. They are reset to logic "0" whenever the MODEM Status Register is read.

Bit 0

Delta Clear To Send (DCTS). Bit 0 indicates that the nCTS input to the chip has changed state since the last time the MSR was read.

Bit 1

Delta Data Set Ready (DDSR). Bit 1 indicates that the nDSR input has changed state since the last time the MSR was read.

Bit 2

Trailing Edge of Ring Indicator (TERI). Bit 2 indicates that the nRI input has changed from logic "0" to logic "1".

Bit 3

Delta Data Carrier Detect (DDCD). Bit 3 indicates that the nDCD input to the chip has changed state.

NOTE: Whenever bit 0, 1, 2, or 3 is set to a logic "1", a MODEM Status Interrupt is generated.

Bit 4

This bit is the complement of the Clear To Send (nCTS) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to nRTS in the MCR.

Bit 5

This bit is the complement of the Data Set Ready (nDSR) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to DTR in the MCR.

Bit 6

This bit is the complement of the Ring Indicator (nRI) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to OUT1 in the MCR.

Bit 7

This bit is the complement of the Data Carrier Detect (nDCD) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to OUT2 in the MCR.

8.8.1.10 Scratchpad Register (SCR)

Address Offset =7H, DLAB =X, READ/WRITE

This 8 bit read/write register has no effect on the operation of the Serial Port. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

8.8.2 Programmable Baud Rate Generator (AND Divisor Latches DLH, DLL)

The Serial Ports contains a programmable Baud Rate Generator that is capable of dividing the internal PLL clock by any divisor from 1 to 65535. The internal PLL clock is divided down to generate a 1.8462MHz frequency for Baud Rates less than 38.4k, a 1.8432MHz frequency for 115.2k, a 3.6864MHz frequency for 230.4k and a 7.3728MHz frequency for 460.8k. This output frequency of the Baud Rate Generator is 16x the Baud rate. Two 8 bit latches store the divisor in 16 bit binary format. These Divisor Latches must be loaded during initialization in order to insure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16 bit Baud counter is immediately loaded. This prevents long counts on initial load. If a 0 is loaded into the BRG registers the output divides the clock by the number 3. If a 1 is loaded the output is the inverse of the input oscillator. If a two is loaded the output is a divide by 2 signal with a 50% duty cycle. If a 3 or greater is loaded the output is low for 2 bits and high for the remainder of the count. The input clock to the BRG is a 1.8462 MHz clock.

Table 8.35 shows the baud rates possible.

8.8.3 Effect Of The Reset on Register File

The Reset Function Table (Table 8.36) details the effect of the Reset input on each of the registers of the Serial Port.

8.8.4 FIFO Interrupt Mode Operation

When the RCVR FIFO and receiver interrupts are enabled (FCR bit 0 = "1", IER bit 0 = "1"), RCVR interrupts occur as follows:

a) The receive data available interrupt will be issued when the FIFO has reached its programmed trigger level; it is cleared as soon as the FIFO drops below its programmed trigger level.

b) The IIR receive data available indication also occurs when the FIFO trigger level is reached. It is cleared when the FIFO drops below the trigger level.

c) The receiver line status interrupt (IIR=06H), has higher priority than the received data available (IIR=04H) interrupt.

d) The data ready bit (LSR bit 0) is set as soon as a character is transferred from the shift register to the RCVR FIFO. It is reset when the FIFO is empty.

When RCVR FIFO and receiver interrupts are enabled, RCVR FIFO timeout interrupts occur as follows:

a) A FIFO timeout interrupt occurs if all the following conditions exist:

- At least one character is in the FIFO.
- The most recent serial character received was longer than 4 continuous character times ago. (If 2 stop bits are programmed, the second one is included in this time delay).
- The most recent CPU read of the FIFO was longer than 4 continuous character times ago.
- This will cause a maximum character received to interrupt issued delay of 160 msec at 300 BAUD with a 12 bit character.

b) Character times are calculated by using the RCLK input for a clock signal (this makes the delay proportional to the baudrate).

c) When a timeout interrupt has occurred it is cleared and the timer reset when the CPU reads one character from the RCVR FIFO.

d) When a timeout interrupt has not occurred the timeout timer is reset after a new character is received or after the CPU reads the RCVR FIFO.

When the XMIT FIFO and transmitter interrupts are enabled (FCR bit 0 = "1", IER bit 1 = "1"), XMIT interrupts occur as follows:

a) The transmitter holding register interrupt (02H) occurs when the XMIT FIFO is empty; it is cleared as soon as the transmitter holding register is written to (1 of 16 characters may be written to the XMIT FIFO while servicing this interrupt) or the IIR is read.

b) The transmitter FIFO empty indications will be delayed 1 character time minus the last stop bit time whenever the following occurs: THRE=1 and there have not been at least two bytes at the same time in the transmitter FIFO since the last THRE=1. The transmitter interrupt after changing FCR0 will be immediate, if it is enabled.

Character timeout and RCVR FIFO trigger level interrupts have the same priority as the current received data available interrupt; XMIT FIFO empty has the same priority as the current transmitter holding register empty interrupt.

8.8.5 FIFO Polled Mode Operation

With FCR bit 0 = "1" resetting IER bits 0, 1, 2 or 3 or all to zero puts the UART in the FIFO Polled mode of operation. Since the RCVR and XMITTER are controlled separately, either one or both can be in the polled mode of operation. In this mode, the user's program will check RCVR and XMITTER status via the LSR. LSR definitions for the FIFO Polled Mode are as follows:

Bit 0=1 as long as there is one byte in the RCVR FIFO.

Bits 1 to 4 specify which error(s) have occurred. Character error status is handled the same way as when in the interrupt mode, the IIR is not affected since EIR bit 2=0.

Bit 5 indicates when the XMIT FIFO is empty.

Bit 6 indicates that both the XMIT FIFO and shift register are empty.

Bit 7 indicates whether there are any errors in the RCVR FIFO.

There is no trigger level reached or timeout condition indicated in the FIFO Polled Mode, however, the RCVR and XMIT FIFOs are still fully capable of holding characters.

Table 8.35 - Baud Rates

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL (Note 8.15)	HIGH SPEED BIT (Note 8.16)
50	2304	0.001	X
75	1536	-	X
110	1047	-	X
134.5	857	0.004	X
150	768	-	X
300	384	-	X
600	192	-	X
1200	96	-	X
1800	64	-	X
2000	58	0.005	X
2400	48	-	X
3600	32	-	X
4800	24	-	X
7200	16	-	X
9600	12	-	X
19200	6	-	X
38400	3	0.030	X
57600	2	0.16	X
115200	1	0.16	X
230400	32770	0.16	1
460800	32769	0.16	1

Note 8.15 The percentage error for all baud rates, except where indicated otherwise, is 0.2%.

Note 8.16 The High Speed bit is located in the Device Configuration Space.

Table 8.36 - Reset Function Table

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Interrupt Enable Register	RESET	All bits low
Interrupt Identification Reg.	RESET	Bit 0 is high; Bits 1 - 7 low
FIFO Control	RESET	All bits low
Line Control Reg.	RESET	All bits low
MODEM Control Reg.	RESET	All bits low
Line Status Reg.	RESET	All bits low except 5, 6 high
MODEM Status Reg.	RESET	Bits 0 - 3 low; Bits 4 - 7 input
TXD1, TXD2	RESET	High
INTRPT (RCVR errs)	RESET/Read LSR	Low
INTRPT (RCVR Data Ready)	RESET/Read RBR	Low
INTRPT (THRE)	RESET/ReadIIR/Write THR	Low
OUT2B	RESET	High
RTSB	RESET	High
DTRB	RESET	High
OUT1B	RESET	High
RCVR FIFO	RESET/	All Bits Low

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
	FCR1*FCR0/_FCR0	
XMIT FIFO	RESET/ FCR1*FCR0/_FCR0	All Bits Low

Table 8.37 - Register Summary for an Individual UART Channel

REGISTER ADDRESS (Note 8.17)	REGISTER NAME	REGISTER SYMBOL	BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
ADDR = 0 DLAB = 0	Receive Buffer Register (Read Only)	RBR	Data Bit 0 (Note 8.18)	Data Bit 1	Data Bit 2	Data Bit 3	Data Bit 4	Data Bit 5	Data Bit 6	Data Bit 7
ADDR = 0 DLAB = 0	Transmitter Holding Register (Write Only)	THR	Data Bit 0	Data Bit 1	Data Bit 2	Data Bit 3	Data Bit 4	Data Bit 5	Data Bit 6	Data Bit 7
ADDR = 1 DLAB = 0	Interrupt Enable Register	IER	Enable Received Data Available Interrupt (ERDAI)	Enable Transmitter Holding Register Empty Interrupt (ETHREI)	Enable Receiver Line Status Interrupt (ELSI)	Enable MODEM Status Interrupt (EMSI)	0	0	0	0
ADDR = 2	Interrupt Ident. Register (Read Only)	IIR	"0" if Interrupt Pending	Interrupt ID Bit	Interrupt ID Bit	Interrupt ID Bit (Note 8.22)	0	0	FIFOs Enabled (Note 8.22)	FIFOs Enabled (Note 8.22)
ADDR = 2	FIFO Control Register (Write Only)	FCR (Note 8.24)	FIFO Enable	RCVR FIFO Reset	XMIT FIFO Reset	DMA Mode Select (Note 8.23)	Reserved	Reserved	RCVR Trigger LSB	RCVR Trigger MSB
ADDR = 3	Line Control Register	LCR	Word Length Select Bit 0 (WLS0)	Word Length Select Bit 1 (WLS1)	Number of Stop Bits (STB)	Parity Enable (PEN)	Even Parity Select (EPS)	Stick Parity	Set Break	Divisor Latch Access Bit (DLAB)
ADDR = 4	MODEM Control Register	MCR	Data Terminal Ready (DTR)	Request to Send (RTS)	OUT1 (Note 8.20)	OUT2 (Note 8.20)	Loop	0	0	0
ADDR = 5	Line Status Register	LSR	Data Ready (DR)	Overrun Error (OE)	Parity Error (PE)	Framing Error (FE)	Break Interrupt (BI)	Transmitter Holding Register (THRE)	Transmitter Empty (TEMT) (Note 8.19)	Error in RCVR FIFO (Note 8.22)
ADDR = 6	MODEM Status Register	MSR	Delta Clear to Send (DCTS)	Delta Data Set Ready (DDSR)	Trailing Edge Ring Indicator (TERI)	Delta Data Carrier Detect (DDCD)	Clear to Send (CTS)	Data Set Ready (DSR)	Ring Indicator (RI)	Data Carrier Detect (DCD)

REGISTER ADDRESS (Note 8.17)	REGISTER NAME	REGISTER SYMBOL	BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
ADDR = 7	Scratch Register (Note 8.21)	SCR	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
ADDR = 0 DLAB = 1	Divisor Latch (LS)	DDL	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
ADDR = 1 DLAB = 1	Divisor Latch (MS)	DLM	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15

Note 8.17 DLAB is Bit 7 of the Line Control Register (ADDR = 3).

Note 8.18 Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

Note 8.19 When operating in the XT mode, this bit will be set any time that the transmitter shift register is empty.

Note 8.20 This bit no longer has a pin associated with it.

Note 8.21 When operating in the XT mode, this register is not available.

Note 8.22 These bits are always zero in the non-FIFO mode.

Note 8.23 Writing a one to this bit has no effect. DMA modes are not supported in this chip.

Note 8.24 The UART1 and UART2 FCR's are shadowed in the UART1 FIFO Control Shadow Register (CR15) and UART2 FIFO Control Shadow Register (CR16).

8.8.6 Notes On Serial Port Operation

8.8.6.1 FIFO Mode Operation

General

The RCVR FIFO will hold up to 16 bytes regardless of which trigger level is selected.

8.8.6.2 TX and RX FIFO Operation

The Tx portion of the UART transmits data through TXD as soon as the CPU loads a byte into the Tx FIFO. **The UART will prevent loads to the Tx FIFO if it currently holds 16 characters.** Loading to the Tx FIFO will again be enabled as soon as the next character is transferred to the Tx shift register. These capabilities account for the largely autonomous operation of the Tx.

The UART starts the above operations typically with a Tx interrupt. The chip issues a Tx interrupt whenever the Tx FIFO is empty and the Tx interrupt is enabled, except in the following instance. Assume that the Tx FIFO is empty and the CPU starts to load it. When the first byte enters the FIFO the Tx FIFO empty interrupt will transition from active to inactive. Depending on the execution speed of the service routine software, the UART may be able to transfer this byte from the FIFO to the shift register before the CPU loads another byte. If this happens, the Tx FIFO will be empty again and typically the UART's interrupt line would transition to the active state. This could cause a system with an interrupt control unit to record a Tx FIFO empty condition, even though the CPU is currently servicing that interrupt. **Therefore, after the first byte has been loaded into the FIFO the UART will wait one serial character transmission time before issuing a new Tx FIFO empty interrupt. This one character Tx interrupt delay will remain active until at least two bytes have the Tx FIFO empties after this condition, the Tx been loaded into the FIFO, concurrently. When interrupt will be activated without a one character delay.**

Rx support functions and operation are quite different from those described for the transmitter. The Rx FIFO receives data until the number of bytes in the FIFO equals the selected interrupt trigger level. At that time if Rx interrupts are enabled, the UART will issue an interrupt to the CPU. The Rx FIFO will continue to store bytes until it holds 16 of them. It will not accept any more data when it is full. Any more data entering the Rx shift register will set the Overrun Error flag. Normally, the FIFO depth and the programmable trigger levels will give the CPU ample time to empty the Rx FIFO before an overrun occurs.

One side-effect of having a Rx FIFO is that the selected interrupt trigger level may be above the data level in the FIFO. This could occur when data at the end of the block contains fewer bytes than the trigger level. No interrupt would be issued to the CPU and the data would remain in the UART. **To prevent the software from having to check for this situation the chip incorporates a timeout interrupt.**

The timeout interrupt is activated when there is a least one byte in the Rx FIFO, and neither the CPU nor the Rx shift register has accessed the Rx FIFO within 4 character times of the last byte. The timeout interrupt is cleared or reset when the CPU reads the Rx FIFO or another character enters it.

These FIFO related features allow optimization of CPU/UART transactions and are especially useful given the higher baud rate capability (256 kbaud).

8.9 Infrared Interface

The SIO10N268 infrared interface provides a two-way wireless communications port using infrared as the transmission medium. Several infrared protocols have been provided in this implementation including IrDA

v1.2 (SIR/FIR), ASKIR, and Consumer IR (Figure 8.8). For more information, consult the SMSC Infrared Communication Controller (IRCC) specification.

The IrDA v1.0 (SIR) and ASKIR formats are driven by the ACE registers found in UART2. The UART2 registers are described in "Serial Port (UART)" section. The base address for UART2 is programmed in CR25, the UART2 Base Address Register (see section CR25 subsection in the Configuration seciton).

The IrDA V1.2 (FIR) and Consumer IR formats are driven by the SCE registers. Descriptions of these registers can be found in the SMSC Infrared Communications Controller Specification. The Base Address for the SCE registers is programmed in CR2B, the SCE Base Address Register (see CR28 subsection in the Configuration section).

8.9.1 IrDA SIR/FIR and ASKIR

IrDA SIR (v1.0) specifies asynchronous serial communication at baud rates up to 115.2Kbps. Each byte is sent serially LSB first beginning with a zero value start bit. A zero is signaled by sending a single infrared pulse at the beginning of the serial bit time. A one is signaled by the absence of an infrared pulse during the bit time. Please refer to "Timing Diagrams" section for the parameters of these pulses and the IrDA waveforms.

IrDA FIR (v1.2) includes IrDA v1.0 SIR and additionally specifies synchronous serial communications at data rates up to 4Mbps.

Data is transferred LSB first in packets that can be up to 2048 bits in length. IrDA v1.2 includes .576Mbps and 1.152Mbps data rates using an encoding scheme that is similar to SIR. The 4Mbps data rate uses a pulse position modulation (PPM) technique.

The ASKIR infrared allows asynchronous serial communication at baud rates up to 19.2Kbps. Each byte is sent serially LSB first beginning with a zero value start bit. A zero is signaled by sending a 500KHz carrier waveform for the duration of the serial bit time. A one is signaled by the absence of carrier during the bit time. Refer to "Timing Diagrams" section for the parameters of the ASKIR waveforms.

8.9.2 Consumer IR

The SIO10N268 Consumer IR interface is a general-purpose Amplitude Shift Keyed encoder/decoder with programmable carrier and bit-cell rates that can emulate many popular TV Remote encoding formats; including, 38KHz PPM, PWM and RC-5. The carrier frequency is programmable from 1.6MHz to 6.25KHz. The bit-cell rate range is 100KHz to 390Hz.

8.9.3 Hardware Interface

The SIO10N268 IR hardware interface is shown in Figure 8.8. This interface supports two types of external FIR transceiver modules. One uses a mode pin (IR Mode) to program the data rate, while the other has a second Rx data pin (IRRX3). The SIO10N268 uses Pin 63 for these functions. Pin 62 has IR Mode and IRRX3 as its first and second alternate function, respectively. These functions are selected through CR29 as shown in Table 8.38.

Table 8.38 - FIR Transceiver Module-Type Select

HP MODE (Note 8.25)	FUNCTION
0	IR Mode
1	IRRX3

Note 8.25 HPMODE is CR29, BIT 4 (see CR29 subsection in the Configuration section). Refer to the Infrared Interface Block Diagram on the following page for HPMODE implementation.

The FAST bit is used to select between the SIR mode and FIR mode receiver, regardless of the transceiver type. If FAST = 1, the FIR mode receiver is selected; if FAST = 0, the SIR mode receiver is selected (Table 8.39).

Table 8.39 - IR Rx Data Pin Selection

CONTROL SIGNALS		INPUTS	
FAST	HPMODE	RX1	RX2
0	X	RX1=RXD2	RX2=IRRX2
X	0	RX1=RXD2	RX2=IRRX2
1	1	RX1=IR Mode/IRRX3	RX2=IR Mode/IRRX3

8.9.4 IR Half Duplex Turnaround Delay Time

If the Half Duplex option is chosen there is an IR Half Duplex Time-out that constrains IRCC direction mode changes. This time-out starts as each bit is transferred and prevents direction mode changes until the time-out expires. The timer is restarted whenever new data arrives in the current direction mode. For example, if data is loaded into the transmit buffer while a character is being received, the transmission will not start until the last bit has been received and the time-out expires. If the start bit of another character is received during this time-out, the timer is restarted after the new character is received. The Half Duplex Time-out is programmable from 0 to 25.5ms in 100µs increments (see section (See subsection CR2D in the Configuration section).

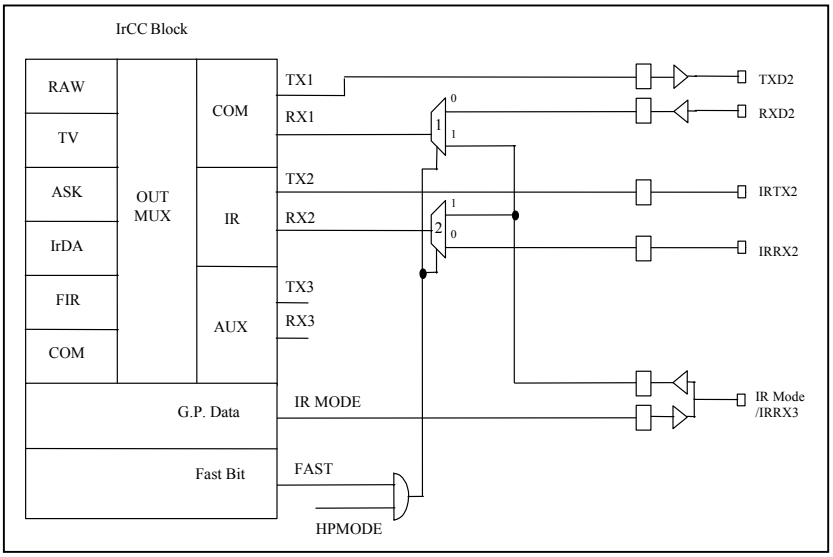


Figure 8.8 - Infrared Interface Block Diagram

8.9.5 IR Transmit Pins

The IR transmit signal may be brought out onto the GP53/TXD2/IRTX pin or the GP21/IRTX2/WDT pin. These pins, which are not powered by VTR, function as described below.

The following defines the acceptable states for the GP53/TXD2/IRTX output pin following a VCC POR or Hard Reset.

- If VCC=0V the GP53/TXD2/IRTX pin will be tristate.
- If VCC>2.4V and TXD2/IRTX functions are selected the following states are possible.
  - If UART2 Power bit = 0 **OR** bits[7:6] IR Output Mux EQUAL '11' at offset CR0A the output will be tristate
  - If UART2 Power bit = 1 **AND** bits[7:6] IR Output Mux EQUAL '00' at offset CR0A **AND** the transmit buffer is empty the output will be set to the inactive state.
  - If UART2 Power bit = 1 **AND** bits[7:6] IR Output Mux EQUAL '00' at offset CR0A **AND** the transmit buffer has data and is ready to transmit the output will reflect the state of the data being transmitted.
  - If UART2 Power bit = 1 **AND** bits[7:6] IR Output Mux EQUAL '01' at offset CR0A the output will be low.
- If VCC>2.4V and GP53 function is selected the pin will reflect the current state of GP53.

The following defines the acceptable states for the GP21/IRTX2/WDT output pin following a VCC POR or Hard Reset.

- If VCC=0V the GP21/IRTX2/WDT pin will be tristate.
- If VCC>2.4V and IRTX2 function is selected the following states are possible.
  - If bits[7:6] IR Output Mux EQUAL '11' at offset CR0A the output will be tristate
  - If UART2 Power bit = 0 AND bits[7:6] IR Output Mux NOT EQUAL '11' at offset CR0A the output will be low.
  - If UART2 Power bit = 1 AND bits[7:6] IR Output Mux EQUAL '01' at offset CR0A AND the transmit buffer is empty the output will be set to the inactive state.
  - If UART2 Power bit = 1 AND bits[7:6] IR Output Mux EQUAL '01' at offset CR0A AND the transmit buffer has data and is ready to transmit the output will reflect the state of the data being transmitted.
  - If UART2 Power bit=1 AND bits[7:6] IR Output Mux EQUAL '00' the output will be low.
- If VCC>2.4V and GP21 function is selected the pin will reflect the current state of GP21.
- If VCC>2.4 and WDT function is selected the pin will reflect the current state of the WDT.

NOTE: The inactive state for GP53/TXD2/IRTX pin or GP21/IRTX2/WDT pin is determined by a combination of the mode selected and the function enabled on the pin. If the TXD2/IRTX or IRTX2 functions are enabled the inactive state is determined by the IR Output Mux bits located in CR0A ECP FIFO Threshold/IR MUX register and the UART Mode register located at CR0C.

8.10 Parallel Port

The SIO10N268 incorporates an IBM XT/AT compatible parallel port. This supports the optional PS/2 type bi-directional parallel port (SPP), the Enhanced Parallel Port (EPP) and the Extended Capabilities Port (ECP) parallel port modes. Refer to the Configuration Registers for information on disabling, power down, changing the base address of the parallel port, and selecting the mode of operation.

The SIO10N268 also provides a mode for support of the floppy disk controller on the parallel port.

The parallel port also incorporates SMSC's ChiProtect circuitry, which prevents possible damage to the parallel port due to printer power-up.

The functionality of the Parallel Port is achieved through the use of eight addressable ports, with their associated registers and control gating. The control and data port are read/write by the CPU, the status port is read/write in the EPP mode. The address map of the Parallel Port is shown below.

DATA PORT	BASE ADDRESS + 00H
STATUS PORT	BASE ADDRESS + 01H
CONTROL PORT	BASE ADDRESS + 02H
EPP ADDR PORT	BASE ADDRESS + 03H
EPP DATA PORT 0	BASE ADDRESS + 04H
EPP DATA PORT 1	BASE ADDRESS + 05H
EPP DATA PORT 2	BASE ADDRESS + 06H
EPP DATA PORT 3	BASE ADDRESS + 07H

The bit map of these registers is:

	D0	D1	D2	D3	D4	D5	D6	D7	Note
DATA PORT	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	**Note 8.26**
STATUS PORT	TMOUT	0	0	nERR	SLCT	PE	nACK	nBUSY	**Note 8.26**
CONTROL PORT	STROBE	AUTOFD	nINIT	SLC	IRQE	PCD	0	0	**Note 8.26**
EPP ADDR PORT	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	**Note 8.27**
EPP DATA PORT 0	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	**Note 8.27**
EPP DATA PORT 1	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	**Note 8.27**
EPP DATA PORT 2	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	**Note 8.27**
EPP DATA PORT 3	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	**Note 8.27**

Note 8.26 These registers are available in all modes.

Note 8.27 These registers are only available in EPP mode.

Table 8.40 - Parallel Port Connector

HOST CONNECTOR	PIN NUMBER	STANDARD	EPP	ECP
1	81	nSTROBE	nWrite	nStrobe
2-9	65-69, 71-73	PD<0:7>	PData<0:7>	PData<0:7>
10	78	nACK	Intr	nAck
11	77	BUSY	nWait	Busy, PeriphAck(3)
12	76	PE	(User Defined)	PError, nAckReverse(3)
13	75	SLCT	(User Defined)	Select
14	80	nALF	nDatastb	nAutoFd, HostAck(3)
15	79	nERROR	(User Defined)	nFault(1) nPeriphRequest(3)

HOST CONNECTOR	PIN NUMBER	STANDARD	EPP	ECP
16	63	nINIT	nRESET	nInit(1) nReverseRqst(3)
17	64	nSLCTIN	nAddrstrb	nSelectIn(1,3)

(1) = Compatible Mode

(3) = High Speed Mode

NOTE: For the cable interconnection required for ECP support and the Slave Connector pin numbers, refer to the IEEE 1284 Extended Capabilities Port Protocol and ISA Standard, Rev. 1.14, July 14, 1993. This document is available from Microsoft.

8.10.1 IBM XT/AT Compatible, Bi-Directional And EPP Modes

8.10.1.1 Data Port

ADDRESS OFFSET = 00H

The Data Port is located at an offset of '00H' from the base address. The data register is cleared at initialization by RESET. During a WRITE operation, the Data Register latches the contents of the internal data bus. The contents of this register are buffered (non inverting) and output onto the PD0 - PD7 ports. During a READ operation in SPP mode, PD0 - PD7 ports are buffered (not latched) and output to the host CPU.

8.10.1.2 Status Port

ADDRESS OFFSET = 01H

The Status Port is located at an offset of '01H' from the base address. The contents of this register are latched for the duration of a read cycle. The bits of the Status Port are defined as follows:

BIT 0 TMOUT - TIME OUT

This bit is valid in EPP mode only and indicates that a 10 usec time out has occurred on the EPP bus. A logic zero means that no time out error has occurred; a logic 1 means that a time out error has been detected.

The means of clearing the TIMEOUT bit is controlled by the TIMEOUT_SELECT bit as follows. The TIMEOUT_SELECT bit is located at bit 2 of CR21.

- If the TIMEOUT_SELECT bit is cleared (‘0’), the TIMEOUT bit is cleared on the trailing edge of the read of the EPP Status Register (default)
- If the TIMEOUT_SELECT bit is set (‘1’), the TIMEOUT bit is cleared on a write of ‘1’ to the TIMEOUT bit.

The TIMEOUT bit is cleared on PCI_RESET regardless of the state of the TIMEOUT_SELECT bit.

BITS 1, 2 - are not implemented as register bits, during a read of the Printer Status Register these bits are a low level.

BIT 3 nERR - nERROR

The level on the nERROR input is read by the CPU as bit 3 of the Printer Status Register. A logic 0 means an error has been detected; a logic 1 means no error has been detected.

BIT 4 SLCT - PRINTER SELECTED STATUS

The level on the SLCT input is read by the CPU as bit 4 of the Printer Status Register. A logic 1 means the printer is on line; a logic 0 means it is not selected.

BIT 5 PE - PAPER END

The level on the PE input is read by the CPU as bit 5 of the Printer Status Register. A logic 1 indicates a paper end; a logic 0 indicates the presence of paper.

BIT 6 nACK - nACKNOWLEDGE

The level on the nACK input is read by the CPU as bit 6 of the Printer Status Register. A logic 0 means that the printer has received a character and can now accept another. A logic 1 means that it is still processing the last character or has not received the data.

BIT 7 nBUSY - nBUSY

The complement of the level on the BUSY input is read by the CPU as bit 7 of the Printer Status Register. A logic 0 in this bit means that the printer is busy and cannot accept a new character. A logic 1 means that it is ready to accept the next character.

8.10.1.3 Control Port

ADDRESS OFFSET = 02H

The Control Port is located at an offset of '02H' from the base address. The Control Register is initialized by the RESET input, bits 0 to 5 only being affected; bits 6 and 7 are hard wired low.

BIT 0 STROBE - STROBE

This bit is inverted and output onto the nSTROBE output.

BIT 1 AUTOFD - AUTOFEED

This bit is inverted and output onto the nAUTOFD output. A logic 1 causes the printer to generate a line feed after each line is printed. A logic 0 means no autofeed.

BIT 2 nINIT - nINITIATE OUTPUT

This bit is output onto the nINIT output without inversion.

BIT 3 SLCTIN - PRINTER SELECT INPUT

This bit is inverted and output onto the nSLCTIN output. A logic 1 on this bit selects the printer; a logic 0 means the printer is not selected.

BIT 4 IRQE - INTERRUPT REQUEST ENABLE

The interrupt request enable bit when set to a high level may be used to enable interrupt requests from the Parallel Port to the CPU. An interrupt request is generated on the IRQ port by a positive going nACK input. When the IRQE bit is programmed low the IRQ is disabled.

BIT 5 PCD - PARALLEL CONTROL DIRECTION

Parallel Control Direction is not valid in printer mode. In printer mode, the direction is always out regardless of the state of this bit. In bi-directional, EPP or ECP mode, a logic 0 means that the printer port is in output mode (write); a logic 1 means that the printer port is in input mode (read).

Bits 6 and 7 during a read are a low level, and cannot be written.

8.10.1.4 EPP Address Port

ADDRESS OFFSET = 03H

The EPP Address Port is located at an offset of '03H' from the base address. The address register is cleared at initialization by RESET. During a WRITE operation, the contents of the internal data bus DB0-DB7 are buffered (non inverting) and output onto the PD0 - PD7 ports. An LPC I/O write cycle causes an EPP ADDRESS WRITE cycle to be performed, during which the data is latched for the duration of the EPP write cycle. During a READ operation, PD0 - PD7 ports are read. An LPC I/O read cycle causes an EPP ADDRESS READ cycle to be performed and the data output to the host CPU, the deassertion of ADDRSTB latches the PData for the duration of the read cycle. This register is only available in EPP mode.

8.10.1.5 EPP Data Port 0

ADDRESS OFFSET = 04H

The EPP Data Port 0 is located at an offset of '04H' from the base address. The data register is cleared at initialization by RESET. During a WRITE operation, the contents of the internal data bus DB0-DB7 are buffered (non inverting) and output onto the PD0 - PD7 ports. An LPC I/O write cycle causes an EPP DATA WRITE cycle to be performed, during which the data is latched for the duration of the EPP write cycle. During a READ operation, PD0 - PD7 ports are read. An LPC I/O read cycle causes an EPP READ cycle to be performed and the data output to the host CPU, the deassertion of DATASTB latches the PData for the duration of the read cycle. This register is only available in EPP mode.

8.10.1.6 EPP Data Port 1

ADDRESS OFFSET = 05H

The EPP Data Port 1 is located at an offset of '05H' from the base address. Refer to EPP DATA PORT 0 for a description of operation. This register is only available in EPP mode.

8.10.1.7 EPP Data Port 2

ADDRESS OFFSET = 06H

The EPP Data Port 2 is located at an offset of '06H' from the base address. Refer to EPP DATA PORT 0 for a description of operation. This register is only available in EPP mode.

8.10.1.8 EPP Data Port 3

ADDRESS OFFSET = 07H

The EPP Data Port 3 is located at an offset of '07H' from the base address. Refer to EPP DATA PORT 0 for a description of operation. This register is only available in EPP mode.

8.10.2 EPP 1.9 Operation

When the EPP mode is selected in the configuration register, the standard and bi-directional modes are also available. If no EPP Read, Write or Address cycle is currently executing, then the PDx bus is in the standard or bi-directional mode, and all output signals (STROBE, AUTOFD, INIT) are as set by the SPP Control Port and direction is controlled by PCD of the Control port.

In EPP mode, the system timing is closely coupled to the EPP timing. For this reason, a watchdog timer is required to prevent system lockup. The timer indicates if more than 10usec have elapsed from the start of the EPP cycle to nWAIT being deasserted (after command). If a time-out occurs, the current EPP cycle is aborted and the time-out condition is indicated in Status bit 0.

During an EPP cycle, if STROBE is active, it overrides the EPP write signal forcing the PDx bus to always be in a write mode and the nWRITE signal to always be asserted.

8.10.2.1 Software Constraints

Before an EPP cycle is executed, the software must ensure that the control register bit PCD is a logic "0" (i.e., a 04H or 05H should be written to the Control port). If the user leaves PCD as a logic "1", and attempts to perform an EPP write, the chip is unable to perform the write (because PCD is a logic "1") and will appear to perform an EPP read on the parallel bus, no error is indicated.

8.10.2.2 EPP 1.9 Write

The timing for a write operation (address or data) is shown in timing diagram EPP Write Data or Address cycle. The chip inserts wait states into the LPC I/O write cycle until it has been determined that the write cycle can complete. The write cycle can complete under the following circumstances:

1) If the EPP bus is not ready (nWAIT is active low) when nDATASTB or nADDRSTB goes active then the write can complete when nWAIT goes inactive high.

2) If the EPP bus is ready (nWAIT is inactive high) then the chip must wait for it to go active low before changing the state of nDATASTB, nWRITE or nADDRSTB. The write can complete once nWAIT is determined inactive.

Write Sequence of Operation

1) The host initiates an I/O write cycle to the selected EPP register.

2) If WAIT is not asserted, the chip must wait until WAIT is asserted.

3) The chip places address or data on PData bus, clears PDIR, and asserts nWRITE.

4) Chip asserts nDATASTB or nADDRSTRB indicating that PData bus contains valid information, and the WRITE signal is valid.

5) Peripheral deasserts nWAIT, indicating that any setup requirements have been satisfied and the chip may begin the termination phase of the cycle.

6) a) The chip deasserts nDATASTB or nADDRSTRB, this marks the beginning of the termination phase. If it has not already done so, the peripheral should latch the information byte now.

   b) The chip latches the data from the internal data bus for the PData bus and drives the sync that indicates that no more wait states are required followed by the TAR to complete the write cycle.

7) Peripheral asserts nWAIT, indicating to the host that any hold time requirements have been satisfied and acknowledging the termination of the cycle.

8) Chip may modify nWRITE and nPDATA in preparation for the next cycle.

8.10.2.3 EPP 1.9 Read

The timing for a read operation (data) is shown in timing diagram EPP Read Data cycle. The chip inserts wait states into the LPC I/O read cycle until it has been determined that the read cycle can complete. The read cycle can complete under the following circumstances:

1) If the EPP bus is not ready (nWAIT is active low) when nDATASTB goes active then the read can complete when nWAIT goes inactive high.

2) If the EPP bus is ready (nWAIT is inactive high) then the chip must wait for it to go active low before changing the state of WRITE or before nDATASTB goes active. The read can complete once nWAIT is determined inactive.

Read Sequence of Operation

1) The host initiates an I/O read cycle to the selected EPP register.

2) If WAIT is not asserted, the chip must wait until WAIT is asserted.

3) The chip tri-states the PData bus and deasserts nWRITE.

4) Chip asserts nDATASTB or nADDRSTRB indicating that PData bus is tri-stated, PDIR is set and the nWRITE signal is valid.

5) Peripheral drives PData bus valid.

6) Peripheral deasserts nWAIT, indicating that PData is valid and the chip may begin the termination phase of the cycle.

7) a) The chip latches the data from the PData bus for the internal data bus and deasserts nDATASTB or nADDRSTRB. This marks the beginning of the termination phase.

   b) The chip drives the sync that indicates that no more wait states are required and drives valid data onto the LAD[3:0] signals, followed by the TAR to complete the read cycle.

8) Peripheral tri-states the PData bus and asserts nWAIT, indicating to the host that the PData bus is tri-stated.

9) Chip may modify nWRITE, PDIR and nPDATA in preparation for the next cycle.

8.10.3 EPP 1.7 Operation

When the EPP 1.7 mode is selected in the configuration register, the standard and bi-directional modes are also available. If no EPP Read, Write or Address cycle is currently executing, then the PDx bus is in the standard or bi-directional mode, and all output signals (STROBE, AUTOFD, INIT) are as set by the SPP Control Port and direction is controlled by PCD of the Control port.

In EPP mode, the system timing is closely coupled to the EPP timing. For this reason, a watchdog timer is required to prevent system lockup. The timer indicates if more than 10usec have elapsed from the start of

the EPP cycle to the end of the cycle. If a time-out occurs, the current EPP cycle is aborted and the time-out condition is indicated in Status bit 0.

8.10.3.1 Software Constraints

Before an EPP cycle is executed, the software must ensure that the control register bits D0, D1 and D3 are set to zero. Also, bit D5 (PCD) is a logic "0" for an EPP write or a logic "1" for and EPP read.

8.10.3.2 EPP 1.7 Write

The timing for a write operation (address or data) is shown in timing diagram EPP 1.7 Write Data or Address cycle. The chip inserts wait states into the I/O write cycle when nWAIT is active low during the EPP cycle. This can be used to extend the cycle time. The write cycle can complete when nWAIT is inactive high.

Write Sequence of Operation

1) The host sets PDIR bit in the control register to a logic "0". This asserts nWRITE.

2) The host initiates an I/O write cycle to the selected EPP register.

3) The chip places address or data on PData bus.

4) Chip asserts nDATASTB or nADDRSTRB indicating that PData bus contains valid information, and the WRITE signal is valid.

5) If nWAIT is asserted, the chip inserts wait states into I/O write cycle until the peripheral deasserts nWAIT or a time-out occurs.

6) The chip drives the final sync, deasserts nDATASTB or nADDRSTRB and latches the data from the internal data bus for the PData bus.

7) Chip may modify nWRITE, PDIR and nPDATA in preparation of the next cycle.

8.10.3.3 EPP 1.7 Read

The timing for a read operation (data) is shown in timing diagram EPP 1.7 Read Data cycle. The chip inserts wait states into the I/O read cycle when nWAIT is active low during the EPP cycle. This can be used to extend the cycle time. The read cycle can complete when nWAIT is inactive high.

Read Sequence of Operation

1) The host sets PDIR bit in the control register to a logic "1". This deasserts nWRITE and tri-states the PData bus.

2) The host initiates an I/O read cycle to the selected EPP register.

3) Chip asserts nDATASTB or nADDRSTRB indicating that PData bus is tri-stated, PDIR is set and the nWRITE signal is valid.

4) If nWAIT is asserted, the chip inserts wait states into the I/O read cycle until the peripheral deasserts nWAIT or a time-out occurs.

5) The Peripheral drives PData bus valid.

6) The Peripheral deasserts nWAIT, indicating that PData is valid and the chip may begin the termination phase of the cycle.

7) The chip drives the final sync and deasserts nDATASTB or nADDRSTRB.

8) Peripheral tri-states the PData bus.

9) Chip may modify nWRITE, PDIR and nPDATA in preparation of the next cycle.

Table 8.41 - EPP Pin Descriptions

EPP SIGNAL	EPP NAME	TYPE	EPP DESCRIPTION
nWRITE	nWrite	O	This signal is active low. It denotes a write operation.
PD<0:7>	Address/Data	I/O	Bi-directional EPP byte wide address and data bus.
INTR	Interrupt	I	This signal is active high and positive edge triggered. (Pass through with no inversion, Same as SPP).
WAIT	nWait	I	This signal is active low. It is driven inactive as a positive acknowledgement from the device that the transfer of data is completed. It is driven active as an indication that the device is ready for the next transfer.
DATASTB	nData Strobe	O	This signal is active low. It is used to denote data read or write operation.
RESET	nReset	O	This signal is active low. When driven active, the EPP device is reset to its initial operational mode.
ADDRSTB	nAddress Strobe	O	This signal is active low. It is used to denote address read or write operation.
PE	Paper End	I	Same as SPP mode.
SLCT	Printer Selected Status	I	Same as SPP mode.
nERR	Error	I	Same as SPP mode.

Note 8.28 SPP and EPP can use 1 common register.

Note 8.29 nWrite is the only EPP output that can be over-ridden by SPP control port during an EPP cycle. For correct EPP read cycles, PCD is required to be a low.

8.10.4 Extended Capabilities Parallel Port

ECP provides a number of advantages, some of which are listed below. The individual features are explained in greater detail in the remainder of this section.

High performance half-duplex forward and reverse channel Interlocked handshake, for fast reliable transfer Optional single byte RLE compression for improved throughput (64:1) Channel addressing for low-cost peripherals Maintains link and data layer separation Permits the use of active output drivers permits the use of adaptive signal timing Peer-to-peer capability.

8.10.5 Vocabulary

The following terms are used in this document:

assert: When a signal asserts it transitions to a "true" state, when a signal deasserts it transitions to a "false" state.

forward: Host to Peripheral communication.

reverse: Peripheral to Host communication

Pword: A port word; equal in size to the width of the LPC interface. For this implementation, PWord is always 8 bits.

1 A high level.

0 A low level.

These terms may be considered synonymous:

- PeriphClk, nAck
- HostAck, nAutoFd
- PeriphAck, Busy
- nPeriphRequest, nFault
- nReverseRequest, nInit
- nAckReverse, PError
- Xflag, Select
- ECPMode, nSelectIn
- HostClk, nStrobe

Reference Document: IEEE 1284 Extended Capabilities Port Protocol and ISA Interface Standard, Rev 1.14, July 14, 1993. This document is available from Microsoft.

The bit map of the Extended Parallel Port registers is:

	D7	D6	D5	D4	D3	D2	D1	D0	NOTE
data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	
ecpAFifo	Addr/RLE	Address or RLE field							Note 8.31
dsr	nBusy	nAck	PError	Select	nFault	0	0	0	Note 8.30
dcr	0	0	Direction	ackIntEn	SelectIn	nInit	autofd	strobe	Note 8.30
cFifo	Parallel Port Data FIFO								Note 8.31
ecpDFifo	ECP Data FIFO								Note 8.31
tFifo	Test FIFO								Note 8.31
cnfgA	0	0	0	1	0	0	0	0	
cnfgB	compress	intrValue	Parallel Port IRQ			Parallel Port DMA			Note 8.32
ecr	MODE			nErrIntrEn	dmaEn	serviceIntr	full	empty	

Note 8.30 These registers are available in all modes.

Note 8.31 All FIFOs use one common 16 byte FIFO.

Note 8.32 The ECP Parallel Port Config Reg B reflects the IRQ and DMA channel selected by the Configuration Registers.

8.10.6 ECP Implementation Standard

This specification describes the standard interface to the Extended Capabilities Port (ECP). All LPC devices supporting ECP must meet the requirements contained in this section or the port will not be supported by Microsoft. For a description of the ECP Protocol, please refer to the IEEE 1284 Extended Capabilities Port Protocol and ISA Interface Standard, Rev. 1.14, July 14, 1993. This document is available from Microsoft.

8.10.6.1 Description

The port is software and hardware compatible with existing parallel ports so that it may be used as a standard LPT port if ECP is not required. The port is designed to be simple and requires a small number of gates to implement. It does not do any "protocol" negotiation, rather it provides an automatic high burst-bandwidth channel that supports DMA for ECP in both the forward and reverse directions.

Small FIFOs are employed in both forward and reverse directions to smooth data flow and improve the maximum bandwidth requirement. The size of the FIFO is 16 bytes deep. The port supports an automatic handshake for the standard parallel port to improve compatibility mode transfer speed.

The port also supports run length encoded (RLE) decompression (required) in hardware. Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times the next byte is to be repeated. Decompression simply intercepts the RLE byte and repeats the following byte the specified number of times. Hardware support for compression is optional.

Table 8.42 - ECP Pin Descriptions

NAME	TYPE	DESCRIPTION
nStrobe	O	During write operations nStrobe registers data or address into the slave on the asserting edge (handshakes with Busy).
PData 7:0	I/O	Contains address or data or RLE data.
nAck	I	Indicates valid data driven by the peripheral when asserted. This signal handshakes with nAutoFd in reverse.
PeriphAck (Busy)	I	This signal deasserts to indicate that the peripheral can accept data. This signal handshakes with nStrobe in the forward direction. In the reverse direction this signal indicates whether the data lines contain ECP command information or data. The peripheral uses this signal to flow control in the forward direction. It is an "interlocked" handshake with nStrobe. PeriphAck also provides command information in the reverse direction.
PError (nAckReverse)	I	Used to acknowledge a change in the direction the transfer (asserted = forward). The peripheral drives this signal low to acknowledge nReverseRequest. It is an "interlocked" handshake with nReverseRequest. The host relies upon nAckReverse to determine when it is permitted to drive the data bus.
Select	I	Indicates printer on line.
nAutoFd (HostAck)	O	Requests a byte of data from the peripheral when asserted, handshaking with nAck in the reverse direction. In the forward direction this signal indicates whether the data lines contain ECP address or data. The host drives this signal to flow control in the reverse direction. It is an "interlocked" handshake with nAck. HostAck also provides command information in the forward phase.

NAME	TYPE	DESCRIPTION
nFault (nPeriphRequest)	I	Generates an error interrupt when asserted. This signal provides a mechanism for peer-to-peer communication. This signal is valid only in the forward direction. During ECP Mode the peripheral is permitted (but not required) to drive this pin low to request a reverse transfer. The request is merely a "hint" to the host; the host has ultimate control over the transfer direction. This signal would be typically used to generate an interrupt to the host CPU.
nInit	O	Sets the transfer direction (asserted = reverse, deasserted = forward). This pin is driven low to place the channel in the reverse direction. The peripheral is only allowed to drive the bi-directional data bus while in ECP Mode and HostAck is low and nSelectIn is high.
nSelectIn	O	Always deasserted in ECP mode.

8.10.6.2 Register Definitions

The register definitions are based on the standard IBM addresses for LPT. All of the standard printer ports are supported. The additional registers attach to an upper bit decode of the standard LPT port definition to avoid conflict with standard ISA devices. The port is equivalent to a generic parallel port interface and may be operated in that mode. The port registers vary depending on the mode field in the ecr. The table below lists these dependencies. Operation of the devices in modes other that those specified is undefined.

Table 8.43 - ECP Register Definitions

NAME	ADDRESS (Note 8.33)	ECP MODES	FUNCTION
data	+000h R/W	000-001	Data Register
ecpAFifo	+000h R/W	011	ECP FIFO (Address)
dsr	+001h R/W	All	Status Register
dcr	+002h R/W	All	Control Register
cFifo	+400h R/W	010	Parallel Port Data FIFO
ecpDFifo	+400h R/W	011	ECP FIFO (DATA)
tFifo	+400h R/W	110	Test FIFO
cnfgA	+400h R	111	Configuration Register A
cnfgB	+401h R/W	111	Configuration Register B
ecr	+402h R/W	All	Extended Control Register

Note 8.33 These addresses are added to the parallel port base address as selected by configuration register or jumpers.

Note 8.34 All addresses are qualified with AEN. Refer to the AEN pin definition.

Table 8.44 - Mode Descriptions

MODE	DESCRIPTION (Note 8.35)
000	SPP mode
001	PS/2 Parallel Port mode
010	Parallel Port Data FIFO mode
011	ECP Parallel Port mode
100	EPP mode (If this option is enabled in the configuration registers)
101	Reserved
110	Test mode
111	Configuration mode

Note 8.35 Refer to ECR Register Description

Data And ecpAFifo Port

ADDRESS OFFSET = 00H

Modes 000 and 001 (Data Port)

The Data Port is located at an offset of '00H' from the base address. The data register is cleared at initialization by RESET. During a WRITE operation, the Data Register latches the contents of the data bus. The contents of this register are buffered (non inverting) and output onto the PD0 - PD7 ports. During a READ operation, PD0 - PD7 ports are read and output to the host CPU.

Mode 011 (ECP FIFO - Address/RLE)

A data byte written to this address is placed in the FIFO and tagged as an ECP Address/RLE. The hardware at the ECP port transmits this byte to the peripheral automatically. The operation of this register is ony defined for the forward direction (direction is 0). Refer to the ECP Parallel Port Forward Timing Diagram, located in the Timing Diagrams section of this data sheet .

Device Status Register (DSR)

ADDRESS OFFSET = 01H

The Status Port is located at an offset of '01H' from the base address. Bits 0 - 2 are not implemented as register bits, during a read of the Printer Status Register these bits are a low level. The bits of the Status Port are defined as follows:

BIT 3 nFault

The level on the nFault input is read by the CPU as bit 3 of the Device Status Register.

BIT 4 Select

The level on the Select input is read by the CPU as bit 4 of the Device Status Register.

BIT 5 PError

The level on the PError input is read by the CPU as bit 5 of the Device Status Register. Printer Status Register.

BIT 6 nAck

The level on the nAck input is read by the CPU as bit 6 of the Device Status Register.

BIT 7 nBusy

The complement of the level on the BUSY input is read by the CPU as bit 7 of the Device Status Register.

Device Control Register (DCR)

ADDRESS OFFSET = 02H

The Control Register is located at an offset of '02H' from the base address. The Control Register is initialized to zero by the RESET input, bits 0 to 5 only being affected; bits 6 and 7 are hard wired low.

BIT 0 STROBE - STROBE

This bit is inverted and output onto the nSTROBE output.

BIT 1 AUTOFD - AUTOFEED

This bit is inverted and output onto the nAUTOFD output. A logic 1 causes the printer to generate a line feed after each line is printed. A logic 0 means no autofeed.

BIT 2 nINIT - nINITIATE OUTPUT

This bit is output onto the nINIT output without inversion.

BIT 3 SELECTIN

This bit is inverted and output onto the nSLCTIN output. A logic 1 on this bit selects the printer; a logic 0 means the printer is not selected.

BIT 4 ackIntEn - INTERRUPT REQUEST ENABLE

The interrupt request enable bit when set to a high level may be used to enable interrupt requests from the Parallel Port to the CPU due to a low to high transition on the nACK input. Refer to the description of the interrupt under Operation, Interrupts.

BIT 5 DIRECTION

If mode=000 or mode=010, this bit has no effect and the direction is always out regardless of the state of this bit. In all other modes, Direction is valid and a logic 0 means that the printer port is in output mode (write); a logic 1 means that the printer port is in input mode (read).

BITS 6 and 7 during a read are a low level, and cannot be written.

cFifo (Parallel Port Data FIFO)

ADDRESS OFFSET = 400h

Mode = 010

Bytes written or DMAed from the system to this FIFO are transmitted by a hardware handshake to the peripheral using the standard parallel port protocol. Transfers to the FIFO are byte aligned. This mode is only defined for the forward direction.

ecpDFifo (ECP Data FIFO)

ADDRESS OFFSET = 400H

Mode = 011

Bytes written or DMAed from the system to this FIFO, when the direction bit is 0, are transmitted by a hardware handshake to the peripheral using the ECP parallel port protocol. Transfers to the FIFO are byte aligned.

Data bytes from the peripheral are read under automatic hardware handshake from ECP into this FIFO when the direction bit is 1. Reads or DMAs from the FIFO will return bytes of ECP data to the system.

tFifo (Test FIFO Mode)

ADDRESS OFFSET = 400H

Mode = 110

Data bytes may be read, written or DMAed to or from the system to this FIFO in any direction. Data in the tFIFO will not be transmitted to the to the parallel port lines using a hardware protocol handshake. However, data in the tFIFO may be displayed on the parallel port data lines.

The tFIFO will not stall when overwritten or underrun. If an attempt is made to write data to a full tFIFO, the new data is not accepted into the tFIFO. If an attempt is made to read data from an empty tFIFO, the last data byte is re-read again. The full and empty bits must always keep track of the correct FIFO state. The tFIFO will transfer data at the maximum ISA rate so that software may generate performance metrics.

The FIFO size and interrupt threshold can be determined by writing bytes to the FIFO and checking the full and serviceIntr bits.

The writeIntrThreshold can be determined by starting with a full tFIFO, setting the direction bit to 0 and emptying it a byte at a time until serviceIntr is set. This may generate a spurious interrupt, but will indicate that the threshold has been reached.

The readIntrThreshold can be determined by setting the direction bit to 1 and filling the empty tFIFO a byte at a time until serviceIntr is set. This may generate a spurious interrupt, but will indicate that the threshold has been reached.

Data bytes are always read from the head of tFIFO regardless of the value of the direction bit. For example if 44h, 33h, 22h is written to the FIFO, then reading the tFIFO will return 44h, 33h, 22h in the same order as was written.

cnfgA (Configuration Register A)

ADDRESS OFFSET = 400H

Mode = 111

This register is a read only register. When read, 10H is returned. This indicates to the system that this is an 8-bit implementation. (PWord = 1 byte)

cnfgB (Configuration Register B)

ADDRESS OFFSET = 401H

Mode = 111

BIT 7 compress

This bit is read only. During a read it is a low level. This means that this chip does not support hardware RLE compression. It does support hardware de-compression!

BIT 6 intrValue

Returns the value of the interrupt to determine possible conflicts.

BITS [5:3] Parallel Port IRQ (read-only)

Refer to Table 8.46.

BITS [2:0] Parallel Port DMA (read-only)

Refer to Table 8.47.

ecr (Extended Control Register)

ADDRESS OFFSET = 402H

Mode = all

This register controls the extended ECP parallel port functions.

BITS 7,6,5

These bits are Read/Write and select the Mode.

BIT 4 nErrIntrEn

Read/Write (Valid only in ECP Mode)

1: Disables the interrupt generated on the asserting edge of nFault.

0: Enables an interrupt pulse on the high to low edge of nFault. Note that an interrupt will be generated if nFault is asserted (interrupting) and this bit is written from a 1 to a 0. This prevents interrupts from being lost in the time between the read of the ecr and the write of the ecr.

BIT 3 dmaEn

Read/Write

1: Enables DMA (DMA starts when serviceIntr is 0).

0: Disables DMA unconditionally.

BIT 2 serviceIntr

Read/Write

1: Disables DMA and all of the service interrupts.

0: Enables one of the following 3 cases of interrupts. Once one of the 3 service interrupts has occurred serviceIntr bit shall be set to a 1 by hardware. It must be reset to 0 to re-enable the interrupts. Writing this bit to a 1 will not cause an interrupt.

case dmaEn=1:

During DMA (this bit is set to a 1 when terminal count is reached).

case dmaEn=0 direction=0:

This bit shall be set to 1 whenever there are writeIntrThreshold or more bytes free in the FIFO.

case dmaEn=0 direction=1:

This bit shall be set to 1 whenever there are readIntrThreshold or more valid bytes to be read from the FIFO.

BIT 1 full

Read only

1: The FIFO cannot accept another byte or the FIFO is completely full.

0: The FIFO has at least 1 free byte.

BIT 0 empty

Read only

1: The FIFO is completely empty.

0: The FIFO contains at least 1 byte of data.

Table 8.45 - Extended Control Register

R/W	MODE
000:	Standard Parallel Port Mode . In this mode the FIFO is reset and common drain drivers are used on the control lines (nStrobe, nAutoFd, nInit and nSelectIn). Setting the direction bit will not tri-state the output drivers in this mode.
001:	PS/2 Parallel Port Mode. Same as above except that direction may be used to tri-state the data lines and reading the data register returns the value on the data lines and not the value in the data register. All drivers have active pull-ups (push-pull).
010:	Parallel Port FIFO Mode. This is the same as 000 except that bytes are written or DMAed to the FIFO. FIFO data is automatically transmitted using the standard parallel port protocol. Note that this mode is only useful when direction is 0. All drivers have active pull-ups (push-pull).
011:	ECP Parallel Port Mode. In the forward direction (direction is 0) bytes placed into the ecpDFifo and bytes written to the ecpAFifo are placed in a single FIFO and transmitted automatically to the peripheral using ECP Protocol. In the reverse direction (direction is 1) bytes are moved from the ECP parallel port and packed into bytes in the ecpDFifo. All drivers have active pull-ups (push-pull).
100:	Selects EPP Mode: In this mode, EPP is selected if the EPP supported option is selected in configuration register CR04 (Bits[1,0] and Bit[6]). All drivers have active pull-ups (push-pull).
101:	Reserved
110:	Test Mode. In this mode the FIFO may be written and read, but the data will not be transmitted on the parallel port. All drivers have active pull-ups (push-pull).
111:	Configuration Mode. In this mode the confgA, confgB registers are accessible at 0x400 and 0x401. All drivers have active pull-ups (push-pull).

Table 8.46 – Extended Control Register (continued)

IRQ SELECTED	cnfgB BITS [5:3]
15	110
14	101
11	100
10	011

Table 8.47 - Extended Control Register (continued)

DMA SELECTED	cnfgB BITS [2:0]
3	011
2	010
1	001
All Others	000

8.10.7 Operation

8.10.7.1 Mode Switching/Software Control

Software will execute P1284 negotiation and all operation prior to a data transfer phase under programmed I/O control (mode 000 or 001). Hardware provides an automatic control line handshake, moving data between the FIFO and the ECP port only in the data transfer phase (modes 011 or 010).

Setting the mode to 011 or 010 will cause the hardware to initiate data transfer.

If the port is in mode 000 or 001 it may switch to any other mode. If the port is not in mode 000 or 001 it can only be switched into mode 000 or 001. The direction can only be changed in mode 001.

8.10.7.2 ECP Operation

Prior to ECP operation the Host must negotiate on the parallel port to determine if the peripheral supports the ECP protocol. This is a somewhat complex negotiation carried out under program control in mode 000.

After negotiation, it is necessary to initialize some of the port bits. The following are required:

- Set Direction = 0, enabling the drivers.
- Set strobe = 0, causing the nStrobe signal to default to the deasserted state.
- Set autoFd = 0, causing the nAutoFd signal to default to the deasserted state.
- Set mode = 011 (ECP Mode)

ECP address/RLE bytes or data bytes may be sent automatically by writing the ecpAFifo or ecpDFifo respectively.

NOTE: All FIFO data transfers are byte wide and byte aligned. Address/RLE transfers are byte-wide and only allowed in the forward direction.

The host may switch directions by first switching to mode = 001, negotiating for the forward or reverse channel, setting direction to 1 or 0, then setting mode = 011. When direction is 1 the hardware shall handshake for each ECP read data byte and attempt to fill the FIFO. Bytes may then be read from the ecpDFifo as long as it is not empty.

ECP transfers may also be accomplished (albeit slowly) by handshaking individual bytes under program control in mode = 001, or 000.

8.10.7.3 Termination from ECP Mode

Termination from ECP Mode is similar to the termination from Nibble/Byte Modes. The host is permitted to terminate from ECP Mode only in specific well-defined states. The termination can only be executed while

the bus is in the forward direction. To terminate while the channel is in the reverse direction, it must first be transitioned into the forward direction.

8.10.7.4 Command/Data

ECP Mode supports two advanced features to improve the effectiveness of the protocol for some applications. The features are implemented by allowing the transfer of normal 8 bit data or 8 bit commands.

When in the forward direction, normal data is transferred when HostAck is high and an 8 bit command is transferred when HostAck is low.

The most significant bit of the command indicates whether it is a run-length count (for compression) or a channel address.

When in the reverse direction, normal data is transferred when PeriphAck is high and an 8 bit command is transferred when PeriphAck is low. The most significant bit of the command is always zero. Reverse channel addresses are seldom used and may not be supported in hardware.

Table 8.48 - Forward Channel Commands (HostAck Low), Reverse Channel Commands (PeripAck Low)

D7	D[6:0]
0	Run-Length Count (0-127) (mode 0011 0X00 only)
1	Channel Address (0-127)

8.10.7.5 Data Compression

The ECP port supports run length encoded (RLE) decompression in hardware and can transfer compressed data to a peripheral. Run length encoded (RLE) compression in hardware is not supported. To transfer compressed data in ECP mode, the compression count is written to the ecpAFifo and the data byte is written to the ecpDFifo.

Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times the next byte is to be repeated. Decompression simply intercepts the RLE byte and repeats the following byte the specified number of times. When a run-length count is received from a peripheral, the subsequent data byte is replicated the specified number of times. A run-length count of zero specifies that only one byte of data is represented by the next data byte, whereas a run-length count of 127 indicates that the next byte should be expanded to 128 bytes. To prevent data expansion, however, run-length counts of zero should be avoided.

8.10.7.6 Pin Definition

The drivers for nStrobe, nAutoFd, nInit and nSelectIn are open-drain in mode 000 and are push-pull in all other modes.

8.10.7.7 LPC Connections

The interface can never stall causing the host to hang. The width of data transfers is strictly controlled on an I/O address basis per this specification. All FIFO-DMA transfers are byte wide, byte aligned and end on a byte boundary. (The PWord value can be obtained by reading Configuration Register A, cnfgA, described in the next section). Single byte wide transfers are always possible with standard or PS/2 mode using program control of the control signals.

8.10.7.8 Interrupts

The interrupts are enabled by serviceIntr in the ecr register.

serviceIntr = 1 Disables the DMA and all of the service interrupts.

serviceIntr = 0 Enables the selected interrupt condition. If the interrupting condition is valid, then the interrupt is generated immediately when this bit is changed from a 1 to a 0. This can occur during Programmed I/O if the number of bytes removed or added from/to the FIFO does not cross the threshold.

An interrupt is generated when:

1) For DMA transfers: When serviceIntr is 0, dmaEn is 1 and the DMA TC cycle is received.

2) For Programmed I/O:

   a) When serviceIntr is 0, dmaEn is 0, direction is 0 and there are writeIntrThreshold or more free bytes in the FIFO. Also, an interrupt is generated when serviceIntr is cleared to 0 whenever there are writeIntrThreshold or more free bytes in the FIFO.

   b) When serviceIntr is 0, dmaEn is 0, direction is 1 and there are readIntrThreshold or more bytes in the FIFO. Also, an interrupt is generated when serviceIntr is cleared to 0 whenever there are readIntrThreshold or more bytes in the FIFO.

3) When nErrIntrEn is 0 and nFault transitions from high to low or when nErrIntrEn is set from 1 to 0 and nFault is asserted.

4) When ackIntEn is 1 and the nAck signal transitions from a low to a high.

8.10.7.9 FIFO Operation

The FIFO threshold is set in the chip configuration registers. All data transfers to or from the parallel port can proceed in DMA or Programmed I/O (non-DMA) mode as indicated by the selected mode. The FIFO is used by selecting the Parallel Port FIFO mode or ECP Parallel Port Mode. (FIFO test mode will be addressed separately.) After a reset, the FIFO is disabled. Each data byte is transferred by a Programmed I/O cycle or DMA cycle depending on the selection of DMA or Programmed I/O mode.

The following paragraphs detail the operation of the FIFO flow control. In these descriptions, <threshold> ranges from 1 to 16. The parameter FIFOTHR, which the user programs, is one less and ranges from 0 to 15.

A low threshold value (i.e. 2) results in longer periods of time between service requests, but requires faster servicing of the request for both read and write cases. The host must be very responsive to the service request. This is the desired case for use with a "fast" system. A high value of threshold (i.e. 12) is used with a "sluggish" system by affording a long latency period after a service request, but results in more frequent service requests.

8.10.7.10 DMA Transfers

DMA transfers are always to or from the ecpDFifo, tFifo or CFifo. DMA utilizes the standard PC DMA services. To use the DMA transfers, the host first sets up the direction and state as in the programmed I/O case. Then it programs the DMA controller in the host with the desired count and memory address. Lastly it sets dmaEn to 1 and serviceIntr to 0. The ECP requests DMA transfers from the host by encoding the LDRQ# pin. The DMA will empty or fill the FIFO using the appropriate direction and mode. When the terminal count in the DMA controller is reached, an interrupt is generated and serviceIntr is asserted,

disabling DMA. In order to prevent possible blocking of refresh requests a DMA cycle shall not be requested for more than 32 DMA cycles in a row. The FIFO is enabled directly by the host initiating a DMA cycle for the requested channel, and addresses need not be valid. An interrupt is generated when a TC cycle is received. (Note: The only way to properly terminate DMA transfers is with a TC cycle.)

DMA may be disabled in the middle of a transfer by first disabling the host DMA controller. Then setting serviceIntr to 1, followed by setting dmaEn to 0, and waiting for the FIFO to become empty or full. Restarting the DMA is accomplished by enabling DMA in the host, setting dmaEn to 1, followed by setting serviceIntr to 0.

8.10.7.11 DMA Mode - Transfers from the FIFO to the Host

NOTE: In the reverse mode, the peripheral may not continue to fill the FIFO if it runs out of data to transfer, even if the chip continues to request more data from the peripheral.

The ECP requests a DMA cycle whenever there is data in the FIFO. The DMA controller responds to the request by reading data from the FIFO. The ECP stop requesting DMA cycles when the FIFO becomes empty or when a TC cycle is received, indicating that no more data is required. If the ECP stops requesting DMA cycles due to the FIFO going empty, then a DMA cycle is requested again as soon as there is one byte in the FIFO. If the ECP stops requesting DMA cycles due to the TC cycle, then a DMA cycle is requested again when there is one byte in the FIFO, and serviceIntr has been re-enabled.

8.10.7.12 Programmed I/O Mode or Non-DMA Mode

The ECP or parallel port FIFOs may also be operated using interrupt driven programmed I/O. Software can determine the writeIntrThreshold, readIntrThreshold, and FIFO depth by accessing the FIFO in Test Mode.

Programmed I/O transfers are to the ecpDFifo at 400H and ecpAFifo at 000H or from the ecpDFifo located at 400H, or to/from the tFifo at 400H. To use the programmed I/O transfers, the host first sets up the direction and state, sets dmaEn to 0 and serviceIntr to 0.

The ECP requests programmed I/O transfers from the host by activating the interrupt. The programmed I/O will empty or fill the FIFO using the appropriate direction and mode.

NOTE: A threshold of 16 is equivalent to a threshold of 15. These two cases are treated the same.

8.10.7.13 Programmed I/O - Transfers from the FIFO to the Host

In the reverse direction an interrupt occurs when serviceIntr is 0 and readIntrThreshold bytes are available in the FIFO. If at this time the FIFO is full it can be emptied completely in a single burst, otherwise readIntrThreshold bytes may be read from the FIFO in a single burst.

readIntrThreshold =(16-<threshold>) data bytes in FIFO

An interrupt is generated when serviceIntr is 0 and the number of bytes in the FIFO is greater than or equal to (16-<threshold>). (If the threshold = 12, then the interrupt is set whenever there are 4-16 bytes in the FIFO). The host must respond to the request by reading data from the FIFO. This process is repeated until the last byte is transferred out of the FIFO. If at this time the FIFO is full, it can be completely emptied in a single burst, otherwise a minimum of (16-<threshold>) bytes may be read from the FIFO in a single burst.

8.10.7.14 Programmed I/O - Transfers from the Host to the FIFO

In the forward direction an interrupt occurs when serviceIntr is 0 and there are writeIntrThreshold or more bytes free in the FIFO. At this time if the FIFO is empty it can be filled with a single burst before the empty bit needs to be re-read. Otherwise it may be filled with writeIntrThreshold bytes.

writeIntrThreshold = (16-<threshold>) free bytes in FIFO

An interrupt is generated when serviceIntr is 0 and the number of bytes in the FIFO is less than or equal to <threshold>. (If the threshold = 12, then the interrupt is set whenever there are 12 or less bytes of data in the FIFO.) The host must respond to the request by writing data to the FIFO. If at this time the FIFO is empty, it can be completely filled in a single burst, otherwise a minimum of (16-<threshold>) bytes may be written to the FIFO in a single burst. This process is repeated until the last byte is transferred into the FIFO.

8.10.8 Parallel Port Floppy Disk Controller

The Floppy Disk Control signals are available optionally on the parallel port pins. When this mode is selected, the parallel port is not available. There are two modes of operation, PPFD1 and PPFD2. These modes can be selected in the Parallel and Serial Extended Setup Register (CR04). PPFD1 has only drive 1 on the parallel port pins; PPFD2 has drive 0 and 1 on the parallel port pins. See the Configuration section for description of the register. The FDC_PP pin can be used to switch the parallel port pins between the FDC and the parallel port functions. See the following sub-section.

The following parallel port pins are read as follows by a read of the parallel port register:

1) Data Register (read) = last Data Register (write)
2) Control Register read as "cable not connected" STROBE, AUTOFD and SLC = 0 and nINIT =1
3) Status Register reads: nBUSY = 0, PE = 0, SLCT = 0, nACK = 1, nERR = 1

The following FDC pins are all in the high impedence state when the PPFDC is actually selected by the drive select register:

1) nWDATA, DENSEL, nHDSEL, nWGATE, nDIR, nSTEP, nDS1, nDS0, nMTR0, nMTR1.
2) If PPFDx is selected, then the parallel port can not be used as a parallel port until "Normal" mode is selected.

The FDC signals are muxed onto the Parallel Port pins as shown in Table 8.50.

For ACPI compliance the FDD pins that are multiplexed onto the Parallel Port function independently of the state of the Parallel Port controller. For example, if the FDC is enabled onto the Parallel Port the multiplexed FDD interface functions normally regardless of the Parallel Port Power control, CR01.2.

Table 8.49 illustrates this functionality.

Table 8.49 - Modified Parallel Port FDD Control

PARALLEL PORT POWER	PARALLEL PORT FDC CONTROL		PARALLEL PORT FDC STATE	PARALLEL PORT STATE
CR01.2	CR04.3	CR04.2		
1	0	0	OFF	ON
0	0	0	OFF	OFF
X	1	X	ON	OFF
	X	1		Note 8.36

Note 8.36 The Parallel Port Control register reads as “Cable Not Connected” when the Parallel Port FDC is enabled; i.e., STROBE = AUTOFD = SLC = 0 and nINIT = 1.

Table 8.50 – FDC Parallel Port Pins

CONNECTOR PIN #	QFP CHIP PIN #	SPP MODE	PIN DIRECTION	FDC MODE	PIN DIRECTION
1	81	nSTROBE	I/O	(nDS0)	I/(O) Note 8.37
2	65	PD0	I/O	nINDEX	I
3	66	PD1	I/O	nTRK0	I
4	67	PD2	I/O	nWP	I
5	68	PD3	I/O	nRDATA	I
6	69	PD4	I/O	nDSKCHG	I
7	71	PD5	I/O	-	-
8	72	PD6	I/O	(nMTR0)	I/(O) Note 8.37
9	73	PD7	I/O	-	-
10	78	nACK	I	nDS1	O
11	77	BUSY	I	nMTR1	O
12	76	PE	I	nWDATA	O
13	75	SLCT	I	nWGATE	O
14	80	nALF	I/O	DRVDEN0	O
15	79	nERROR	I	nHDSEL	O
16	63	nINIT	I/O	nDIR	O
17	64	nSLCTIN	I/O	nSTEP	O

Note 8.37 These pins are outputs in mode PPFD2, inputs in mode PPFD1.

8.10.8.1 FDC on Parallel Port Pin

The “floppy on the parallel port” pin function, FDC_PP, is muxed onto GP11. This pin function can be used to switch the parallel port pins between the FDC and the parallel port. The FDC_PP pin can generate a PME and an SMI by enabling GP11 in the appropriate PME and SMI enable registers (bit[1] of PME_EN1 and bit[1] of SMI_EN1 – see the Runtime Registers section). This pin generates an SMI and PME on both a low-to-high and a high-to-low edge.

The pin function for GP11 is selectable in the GPIO Alternate Function Select register 1 located at offset CR44. GPIO Polarity Register 1 at offset CR32 controls the polarity of the GP11 pin. When the FDC_PP function is selected, the pin must also be selected as an input via bit[1] of the GPIO Direction Register 1 located at offset CR31.

If the Floppy_PP bits, CR21 bits[1:0] = 01 or 10, and the FDC_PP function is selected on GP11, then the default functionality (non-inverted polarity) for this pin is as follows: when the pin is low, the parallel port pins are used for a floppy disk controller; when the pin is high, the parallel port pins are used for a parallel port. The polarity bit controls the state of the pin.

If the Floppy_PP bits, CR21 bits[1:0]=00 then the pin is not used to switch the parallel port pins between the FDC and the parallel port, even if the FDC_PP function is selected on GP11. See the Configuration section for register description.

NOTE: When the floppy is selected on the parallel port, the parallel port IRQ, SMI and the parallel port DRQ will not come out of the part.

8.11 Watchdog Timer

The SIO10N268's Watchdog Timer (WDT) has a programmable time-out ranging from 1 to 255 minutes with one minute resolution, or 1 to 255 seconds with 1 second resolution. The units of the WDT timeout value are selected via bit[7] of the WDT_TIMEOUT register (Runtime Register at offset 0x11). The WDT time-out value is set through the WDT_VAL Runtime register. Setting the WDT_VAL register to 0x00 disables the WDT function (this is its power on default). Setting the WDT_VAL to any other non-zero value will cause the WDT to reload and begin counting down from the value loaded. When the WDT count value reaches zero the counter stops and sets the Watchdog time-out status bit in the WDT_CTRL Runtime register. Note: Regardless of the current state of the WDT, the WDT time-out status bit can be directly set or cleared by the Host CPU.

The Watchdog Timer may be configured to generate an interrupt on the rising edge of the Time-out status bit. This interrupt can be used to generate an IO_PME#, an IO_SMI#, a signal on the WDT output pin, or it may be mapped onto the Serial IRQ stream. The following list describes the registers used to enable these events.

NOTE: The WDT, PME, and SMI registers are located in the Runtime Register block.

NOTE: The WDT defaults to generating an active high signal. The polarity of this output may be inverted to generate an active low signal through bit[1] GP21 located in GPIO Polarity Register 2 at offset CR34.

Four methods of enabling Watchdog Timer interrupt events:

1) The WDT can generate an IO_PME#. If a watchdog timer event occurs the WDT status bit in the PME_STS2 register at offset 0x03 will be set. If bit[0] PME_En in the PME_En registers at offset 0x01 is set to '1' and bit[7] WDT in the PME_EN2 register at offset 0x06 is set to '1' an interrupt will be generated on the IO_PME# pin.
2) The WDT can generate an IO_SMI#. If a watchdog timer event occurs the WDT status bit in the SMI_STS3 register at offset 0x18 will be set. If bits[5:4] GP12 Alternate Function Select in the GPIO Alternate Function Select Register 1 at offset CR44 are set to '01' and bit[0]EN_WDT in the SMI_EN3 at offset 0x19 is set to '1' an interrupt will be generated on the IO_SMI# pin.
3) The WDT can generate a signal on the GP21/IRTX2/WDT pin. If a watchdog timer event occurs and bits[3:2] GP21 Alternate Function Select in the GPIO Alternate Function Select Register 3 at offset CR46 are set to '10' an interrupt will be generated on the WDT pin.
4) The WDT can generate an interrupt on the Serial IRQ stream. If a watchdog timer event occurs and bits[7:4] WDT Interrupt Mapping located in the WDT_CFG register at offset 0x13 are programmed to a value other than '0000' an interrupt will be generated on the SER_IRQ output pin. See section 8.14 Serial IRQ on page 135 for a description of generating interrupts on the SER_IRQ pin.

The host may force a Watchdog time-out to occur by writing a "1" to bit 2 of the WDT_CTRL (Force WD Time-out) Runtime register. Writing a "1" to this bit forces the WDT count value to zero and sets bit 0 of the WDT_CTRL (Watchdog Status). Bit 2 of the WDT_CTRL is self-clearing.

See Chapter 9 Runtime Registers for description of these registers.

8.12 LED Functionality

The SIO10N268 provides LED functionality on two pins:

- GP13/IRQIN1/LED1
- GP23/LED2/IRQIN2

The LED logic and supporting registers are powered by VTR. The LED1 pin is powered by VCC and the LED2 pin is powered by VTR. These pins can be configured to turn an LED on and off and blink

independent of each other through the LED1 and LED2 runtime registers at offset 0x15 and 0x16, when the device is powered by VCC. See section Chapter 9 Runtime Registers for a description of these registers.

The LED2 pin (GP23) is capable of controlling an LED while the device is under VTR power with VCC removed. In order to control an LED while the part is under VTR power, the GPIO pin must have been configured for the LED2 function while the device was powered by VCC.

NOTE: The LED2 pin will not support the blink function under VTR power (VCC removed) if an external 32kHz clock source is not connected.

NOTE: LED1 and LED2 may be configured for either open drain or push-pull buffer type. In the case of open-drain buffer type, the pin is capable of sinking current to control the LED. In the case of push-pull buffer type the part will source current.

8.13 Power Management

Power management capabilities are provided for the following logical devices: floppy disk, UART 1, UART 2, UART 3, UART 4, and the parallel port. For each logical device, two types of power management are provided: direct powerdown and auto powerdown.

8.13.1 FDC Power Management

Direct power management is controlled by Bit[3] in CR00. Refer to the Configuration section for more information.

Auto Power Management is enabled by Bit[7] in CR07. When set, this bit allows FDC to enter powerdown when all of the following conditions have been met:

1) The motor enable pins of register 3F2H are inactive (zero).
2) The part must be idle; MSR=80H and INT = 0 (INT may be high even if MSR = 80H due to polling interrupts).
3) The head unload timer must have expired.
4) The Auto powerdown timer (10msec) must have timed out.

An internal timer is initiated as soon as the auto powerdown command is enabled. The part is then powered down when all the conditions are met.

Disabling the auto powerdown mode cancels the timer and holds the FDC block out of auto powerdown.

NOTE: **At least 8us delay should be added when exiting FDC Auto Powerdown mode. If the operating environment is such that this delay cannot be guaranteed, the auto powerdown mode should not be used and Direct powerdown mode should be used instead. The Direct powerdown mode requires at least 8us delay at 250K bits/sec configuration and 4us delay at 500K bits/sec. The delay should be added so that the internal microcontroller can prepare itself to accept commands. See SMSC Application Note: Application Considerations When Using the Powerdown Feature of SMSC Floppy Disk Controllers.**

8.13.1.1 DSR From Powerdown

If DSR powerdown is used when the part is in auto powerdown, the DSR powerdown will override the auto powerdown. However, when the part is awakened from DSR powerdown, the auto powerdown will once again become effective.

8.13.1.2 Wake Up From Auto Powerdown

If the part enters the powerdown state through the auto powerdown mode, then the part can be awakened by reset or by appropriate access to certain registers.

If a hardware or software reset is used then the part will go through the normal reset sequence. If the access is through the selected registers, then the FDC resumes operation as though it was never in powerdown. Besides activating the PCI_RESET# pin or one of the software reset bits in the DOR or DSR, the following register accesses will wake up the part:

1) Enabling any one of the motor enable bits in the DOR register (reading the DOR does not awaken the part).
2) A read from the MSR register.
3) A read or write to the Data register.

Once awake, the FDC will reinitiate the auto powerdown timer for 10 ms. The part will powerdown again when all the powerdown conditions are satisfied.

8.13.1.3 Register Behavior

Table 8.51 illustrates the AT and PS/2 (including Model 30) configuration registers available and the type of access permitted. In order to maintain software transparency, access to all the registers must be maintained. As Table 8.51 shows, two sets of registers are distinguished based on whether their access results in the part remaining in powerdown state or exiting it.

Access to all other registers is possible without awakening the part. These registers can be accessed during powerdown without changing the status of the part. A read from these registers will reflect the true status as shown in the register description in the FDC description. A write to the part will result in the part retaining the data and subsequently reflecting it when the part awakens. Accessing the part during powerdown may cause an increase in the power consumption by the part. The part will revert back to its low power mode when the access has been completed.

8.13.1.4 Pin Behavior

The SIO10N268 is specifically designed for systems in which power conservation is a primary concern. This makes the behavior of the pins during powerdown very important.

The pins of the SIO10N268 can be divided into two major categories: system interface and floppy disk drive interface. The floppy disk drive pins are disabled so that no power will be drawn through the part as a result of any voltage applied to the pin within the part's power supply range. Most of the system interface pins are left active to monitor system accesses that may wake up the part.

Table 8.51 - PC/AT and PS/2 Available Registers

	AVAILABLE REGISTERS		
BASE + ADDRESS	**PC-AT**	**PS/2 (MODEL 30)**	**ACCESS PERMITTED**
Access to these registers DOES NOT wake up the part			
00H	----	SRA	R
01H	----	SRB	R
02H	DOR (**Note 8.38**)	DOR (**Note 8.38**)	R/W
03H	---	---	---
04H	DSR (**Note 8.38**)	DSR (**Note 8.38**)	W

	AVAILABLE REGISTERS		
BASE + ADDRESS	PC-AT	PS/2 (MODEL 30)	ACCESS PERMITTED
06H	---	---	---
07H	DIR	DIR	R
07H	CCR	CCR	W
Access to these registers wakes up the part			
04H	MSR	MSR	R
05H	Data	Data	R/W

Note 8.38 Writing to the DOR or DSR does not wake up the part, however, writing any of the motor enable bits or doing a software reset (via DOR or DSR reset bits) will wake up the part.

8.13.1.5 System Interface Pins

Neither the LPC or ISA interface pins are effected by the direct powerdown or auto powerdown states.

8.13.1.6 FDD Interface Pins

All pins in the FDD interface which can be connected directly to the floppy disk drive itself are either DISABLED or TRISTATED.

Pins used for local logic control or part programming are unaffected. Table 8.52 depicts the state of the floppy disk drive interface pins in the powerdown state.

Table 8.52 - State of Floppy Disk Drive Interface Pins in Powerdown

FDD PINS	STATE IN AUTO POWERDOWN
INPUT PINS	
nRDATA	Input
nWRTPRT	Input
nTRK0	Input
nINDEX	Input
nDSKCHG	Input
OUTPUT PINS	
nMTR0	Tristated
nDS0	Tristated
nDIR	Tristated
nSTEP	Tristated
nWDATA	Tristated
nWGATE	Tristated
nHDSEL	Tristated
DRVDEN[0:1]	Tristated

8.13.2 UART Power Management

Direct power management is controlled by CR02. Refer to the Configuration section for more information.

Auto Power Management may be enabled by the UART1, UART2, UART3, or UART4 enable bits in CR07. When set, these bits allow the following auto power management operations:

1) The transmitter enters auto powerdown when the transmit buffer and shift register are empty.
2) The receiver enters powerdown when the following conditions are all met:
   a) Receive FIFO is empty
   b) The receiver is waiting for a start bit.

NOTE: While in powerdown the Ring Indicator interrupt is still valid and transitions when the RI input changes.

8.13.2.1 Exit Auto Powerdown

The transmitter exits powerdown on a write to the XMIT buffer. The receiver exits auto powerdown when RXDx changes state.

8.13.3 Parallel Port

Direct power management is controlled by Bit[2] in CR01. Refer to the Configuration section for more information.

Auto Power Management is enabled by Bit[4] in CR07. When set, this bit allows the ECP or EPP logical parallel port blocks to be placed into powerdown when not being used.

The EPP logic is in powerdown under any of the following conditions:

1) EPP is not enabled in the configuration registers.
2) EPP is not selected through ecr while in ECP mode.

The ECP logic is in powerdown under any of the following conditions:

1) ECP is not enabled in the configuration registers.
2) SPP, PS/2 Parallel port or EPP mode is selected through ecr while in ECP mode.

8.13.3.1 Exit Auto Powerdown

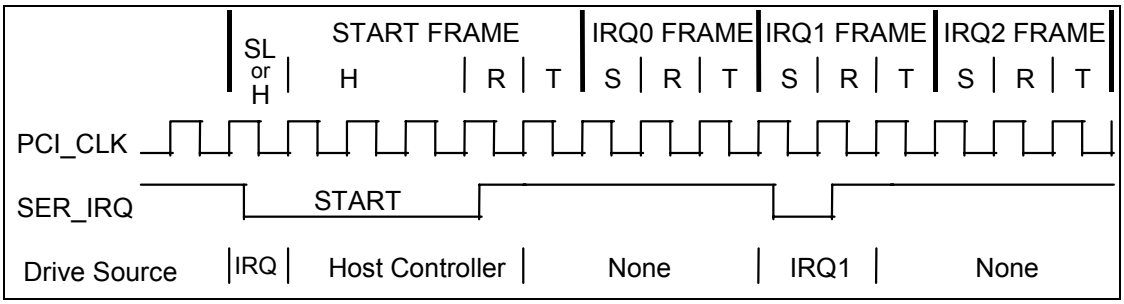
The parallel port logic can change powerdown modes when the ECP mode is changed through the ecr register or when the parallel port mode is changed through the configuration registers.

8.14 Serial IRQ

The SIO10N268 supports the serial interrupt to transmit interrupt information to the host system. The serial interrupt scheme adheres to the Serial IRQ Specification for PCI Systems, Version 6.0. The PCI_CLK, SER_IRQ and nCLKRUN pins are used for this interface. The Serial IRQ/CLKRUN Enable bit D7 in CR29 activates the serial interrupt interface.

8.14.1 Timing Diagrams For SER_IRQ Cycle

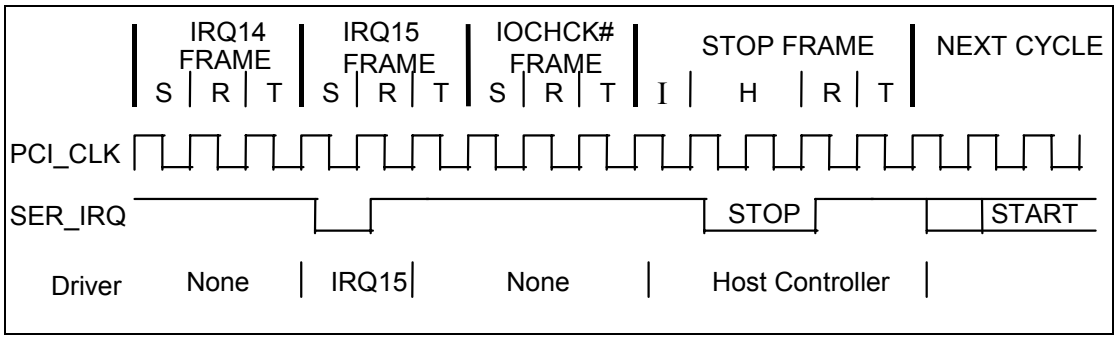
a) Start Frame timing with source sampled a low pulse on IRQ1



NOTE: H=Host Control; R=Recovery; T=Turn-Around; SL=Slave Control; S=Sample

Note 8.39 Start Frame pulse can be 4-8 clocks wide depending on the location of the device in the PCI bridge hierarchy in a synchronous bridge design.

a) Stop Frame Timing with Host using 17 SER_IRQ sampling period.



NOTE: H=Host Control; R=Recovery; T=Turn-Around; S=Sample; I=Idle

Note 8.40 Stop pulse is 2 clocks wide for Quiet mode, 3 clocks wide for Continuous mode.

Note 8.41 There may be none, one or more Idle states during the Stop Frame.

Note 8.42 The next SER_IRQ cycle's Start Frame pulse may or may not start immediately after the turn-around clock of the Stop Frame.

8.14.1.1 SER_IRQ Cycle Control

There are two modes of operation for the SER_IRQ Start Frame.

1) Quiet (Active) Mode:

Any device may initiate a Start Frame by driving the SER_IRQ low for one clock, while the SER_IRQ is Idle. After driving low for one clock the SER_IRQ is immediately tri-stated without at any time driving high. A Start Frame may not be initiated while the SER_IRQ is Active. The SER_IRQ is Idle between Stop and Start Frames. The SER_IRQ is Active between Start and Stop Frames. This mode of operation allows the SER_IRQ to be Idle when there are no IRQ/Data transitions which should be most of the time.

Once a Start Frame has been initiated the Host Controller will take over driving the SER_IRQ low in the next clock and will continue driving the SER_IRQ low for a programmable period of three to seven clocks. This makes a total low pulse width of four to eight clocks. Finally, the Host Controller will drive the SER_IRQ back high for one clock, then tri-state.

Any SER_IRQ Device (i.e., The SIO10N268) which detects any transition on an IRQ/Data line for which it is responsible must initiate a Start Frame in order to update the Host Controller unless the SER_IRQ is already in an SER_IRQ Cycle and the IRQ/Data transition can be delivered in that SER_IRQ Cycle.

2) Continuous (Idle) Mode:

Only the Host controller can initiate a Start Frame to update IRQ/Data line information. All other SER_IRQ agents become passive and may not initiate a Start Frame. SER_IRQ will be driven low for four to eight clocks by Host Controller. This mode has two functions. It can be used to stop or idle the SER_IRQ or the Host Controller can operate SER_IRQ in a continuous mode by initiating a Start Frame at the end of every Stop Frame.

An SER_IRQ mode transition can only occur during the Stop Frame. Upon reset, SER_IRQ bus is defaulted to Continuous mode, therefore only the Host controller can initiate the first Start Frame. Slaves must continuously sample the Stop Frames pulse width to determine the next SER_IRQ Cycle's mode.

8.14.1.2 SER_IRQ Data Frame

Once a Start Frame has been initiated, the SIO10N268 will watch for the rising edge of the Start Pulse and start counting IRQ/Data Frames from there. Each IRQ/Data Frame is three clocks: Sample phase, Recovery phase, and Turn-around phase. During the Sample phase the SIO10N268 drives the SER_IRQ low, if and only if, its last detected IRQ/Data value was low. If its detected IRQ/Data value is high, SER_IRQ is left tri-stated. During the Recovery phase the SIO10N268 drives the SER_IRQ high, if and only if, it had driven the SER_IRQ low during the previous Sample Phase. During the Turn-around Phase the SIO10N268 tri-states the SER_IRQ. The SIO10N268 will drive the SER_IRQ line low at the appropriate sample point if its associated IRQ/Data line is low, regardless of which device initiated the Start Frame.

The Sample Phase for each IRQ/Data follows the low to high transition of the Start Frame pulse by a number of clocks equal to the IRQ/Data Frame times three, minus one. (e.g. The IRQ5 Sample clock is the sixth IRQ/Data Frame, (6 x 3) - 1 = 17th clock after the rising edge of the Start Pulse).

Table 8.53 - SER_IRQ Sampling Periods

SER_IRQ PERIOD	SIGNAL SAMPLED	# OF CLOCKS PAST START
1	Not Used	2
2	IRQ1	5
3	IO_SMI#/IRQ2	8
4	IRQ3	11
5	IRQ4	14
6	IRQ5	17
7	IRQ6	20
8	IRQ7	23
9	IRQ8	26
10	IRQ9	29
11	IRQ10	32
12	IRQ11	35
13	IRQ12	38
14	IRQ13	41
15	IRQ14	44
16	IRQ15	47

The SER_IRQ data frame supports IRQ2 from a logical device on Period 3, which can be used for the System Management Interrupt (nSMI). When using Period 3 for IRQ2 the user should mask off the SMI via the SMI Enable Register. Likewise, when using Period 3 for nSMI the user should not configure any logical devices as using IRQ2.

SER_IRQ Period 14 is used to transfer IRQ13. Logical devices FDC, Parallel Port, Serial Port 1, Serial Port 2, Serial Port 3, Serial Port 4, and WDT have IRQ13 as a choice for their primary interrupt.

The SMI is enabled onto the SMI frame of the Serial IRQ via bit 6 of SMI Enable Register 2 and onto the IO_SMI# pin via bit 7 of the SMI Enable Register 2.

The following devices may be mapped into the Serial IRQ stream.

- FDC
- Parallel Port
- Serial Port 1
- Serial Port 2
- Serial Port 3
- Serial Port 4
- WDT

8.14.1.3 Stop Cycle Control

Once all IRQ/Data Frames have completed the Host Controller will terminate SER_IRQ activity by initiating a Stop Frame. Only the Host Controller can initiate the Stop Frame. A Stop Frame is indicated when the SER_IRQ is low for two or three clocks. If the Stop Frame's low time is two clocks then the next SER_IRQ Cycle's sampled mode is the Quiet mode; and any SER_IRQ device may initiate a Start Frame in the second clock or more after the rising edge of the Stop Frame's pulse. If the Stop Frame's low time is three clocks then the next SER_IRQ Cycle's sampled mode is the Continuos mode; and only the Host Controller may initiate a Start Frame in the second clock or more after the rising edge of the Stop Frame's pulse.

8.14.1.4 Latency

Latency for IRQ/Data updates over the SER_IRQ bus in bridge-less systems with the minimum Host supported IRQ/Data Frames of seventeen, will range up to 96 clocks (3.84μS with a 25MHz PCI Bus or 2.88uS with a 33MHz PCI Bus). If one or more PCI to PCI Bridge is added to a system, the latency for IRQ/Data updates from the secondary or tertiary buses will be a few clocks longer for synchronous buses, and approximately double for asynchronous buses.

8.14.1.5 EOI/ISR Read Latency

Any serialized IRQ scheme has a potential implementation issue related to IRQ latency. IRQ latency could cause an EOI or ISR Read to precede an IRQ transition that it should have followed. This could cause a system fault. The host interrupt controller is responsible for ensuring that these latency issues are mitigated. The recommended solution is to delay EOIs and ISR Reads to the interrupt controller by the same amount as the SER_IRQ Cycle latency in order to ensure that these events do not occur out of order.

8.14.1.6 AC/DC Specification Issue

All SER_IRQ agents must drive / sample SER_IRQ synchronously related to the rising edge of PCI bus clock. The SER_IRQ pin uses the electrical specification of PCI bus. Electrical parameters will follow PCI spec. section 4, sustained tri-state.

8.14.1.7 Reset and Initialization

The SER_IRQ bus uses PCI_RESET# as its reset signal. The SER_IRQ pin is tri-stated by all agents while PCI_RESET# is active. With reset, SER_IRQ Slaves are put into the (continuous) IDLE mode. The Host

Controller is responsible for starting the initial SER_IRQ Cycle to collect system's IRQ/Data default values. The system then follows with the Continuous/Quiet mode protocol (Stop Frame pulse width) for subsequent SER_IRQ Cycles. It is Host Controller's responsibility to provide the default values to 8259's and other system logic before the first SER_IRQ Cycle is performed. For SER_IRQ system suspend, insertion, or removal application, the Host controller should be programmed into Continuous (IDLE) mode first. This is to guarantee SER_IRQ bus is in IDLE state before the system configuration changes.

8.14.2 Routable IRQ Inputs

The routable IRQ input (IRQINx) functions are on pins 53 (GP13/IRQIN1/LED1), 20 (GP23/nLED2/IRQIN2), and 60 (GP20/IRRX2/IRQIN3). The IRQINx pin's IRQ time slot in the Serial IRQ stream is selected via a 4-bit control register for each IRQIN function (CR29 for IRQIN1, CR2A for IRQIN2 and IRQIN3). A value of 0000 disables the IRQ function.

NOTE: In order to use an IRQ for one of the IRQINx inputs that are muxed on the GPIO pins, the corresponding IRQ must not be used for any of the devices in the SIO10N268. Otherwise contention may occur.

IRQIN1, IRQIN2, and IRQIN3 are capable of generating PME wake events. If an IRQINx pin generates an event, the associated PME Wake Status bit will be set to '1'. The following is a list of the PME status and enable bits associated with the IRQINx pins.

- IRQIN1 will generate an event on bit[3] GP13 of the PME_STS1 register at offset 0x02. If bit[3] GP13 of the PME_EN1 register at offset 0x05 is set to '1' and the PME_EN bit is set to '1' in the PME_EN register offset 0x01 the IO_PME# pin will be asserted.
- IRQIN2 will generate an event on bit[5] GP23 of the PME_STS2 register at offset 0x03. If bit[5] GP23 of the PME_EN2 register at offset 0x06 is set to '1' and the PME_EN bit is set to '1' in the PME_EN register offset 0x01 the IO_PME# pin will be asserted.
- IRQIN3 will generate an event on bit[2] GP20 of the PME_STS2 register at offset 0x03. If bit[2] GP20 of the PME_EN2 register at offset 0x06 is set to '1' and the PME_EN bit is set to '1' in the PME_EN register offset 0x01 the IO_PME# pin will be asserted.

IRQIN1 and IRQIN2 are capable of generating SMI events. If an IRQINx pin generates an event, the associated SMI Status bit will be set to '1'. The following is a list of the SMI status and enable bits associated with the IRQINx pins.

- IRQIN1 will generate an event on bit[3] GP13 of the SMI_STS1 register at offset 0x08. If bit[3] GP13 of the SMI_EN1 register at offset 0x0A is set to '1' the IO_SMI# pin will be asserted.
- IRQIN2 will generate an event on bit[4] GP23 of the SMI_STS2 register at offset 0x09. If bit[4] GP23 of the SMI_EN2 register at offset 0x0B is set to '1' the IO_SMI# pin will be asserted.

NOTE: IRQIN3 is not capable of generating an SMI event. The edge is programmable through the polarity bit of the GPIO control register.

Application Note:

If GPIO function is selected on GP13/IRQIN1, GP23/nLED2/IRQIN2, or GP20/IRRX2/IRQIN3 pins and if IRQ is selected using the routing registers (CR29 for IRQIN1 and CR2A for IRQIN2 and IRQIN3), IRQs will be generated on the Serial IRQ stream. The state of the GPIO pins will be reflected on the serial IRQ stream. The IRQ selection bits should be '0000' in the IRQ routing registers when GPIO functions are used. These IRQ selection bits default to '0000' on VCC POR.

8.15 PCI CLKRUN Support

8.15.1 Overview

The SIO10N268 supports the PCI CLKRUN# signal. CLKRUN# is used to indicate the PCI clock status as well as to request that a stopped clock be started. The SIO10N268 CLKRUN# signal is on pin number 28. See Figure 8.9 for an example of a typical system implementation using CLKRUN#.

If the SIO10N268 SIRQ_CLKRUN_EN signal is disabled, it will disable the CLKRUN# support related to LDRQ# in addition to disabling the SER_IRQ and the CLKRUN# associated with SER_IRQ.

CLKRUN# is an open drain output and an input. Refer to the *PCI Mobile Design Guide Rev 1.0* for a description of the CLKRUN# function.

8.15.2 CLKRUN# for Serial IRQ

The SIO10N268 supports the PCI CLKRUN# signal for the Serial IRQs. If an SIO interrupt occurs while the PCI clock is stopped, CLKRUN# is asserted before the serial interrupt signal is driven active.

See section 8.15.4 Using CLKRUN# below for more details.

8.15.3 CLKRUN# for LDRQ#

CLKRUN# support is also provided in the SIO10N268 for the LDRQ# signal. If a device requests DMA service while the PCI clock is stopped, CLKRUN# is asserted to restart the PCI clock. This is required to drive the LDRQ# signal active.

See section 8.15.4 Using CLKRUN# below for more details.

8.15.4 Using CLKRUN#

If CLKRUN# is sampled “high”, the PCI clock is stopped or stopping. If CLKRUN# is sampled “low”, the PCI clock is starting or started (running). If a device in the SIO10N268 asserts or de-asserts an interrupt or asserts a DMA request, and CLKRUN# is sampled “high”, the SIO10N268 requests the restoration of the clock by asserting the CLKRUN# signal asynchronously (Table 8.54). The SIO10N268 holds CLKRUN# low until it detects two rising edges of the clock. After the second clock edge, the SIO10N268 disables the open drain driver (Figure 8.10).

The SIO10N268 will not assert CLKRUN# under any conditions if SIRQ_CLKRUN_EN is inactive (“0”). The SIRQ_CLKRUN_EN bit is D7 in CR29.

The SIO10N268 will not assert CLKRUN# if it is already driven low by the central resource; i.e., the PCI CLOCK GENERATOR in Figure 8.9. The SIO10N268 will not assert CLKRUN# unless the line has been deasserted for two successive clocks; i.e., before the clock was stopped (Figure 8.10).

Table 8.54 - SIO10N268 CLKRUN# Function

SIRQ_CLKRUN_EN	INTERNAL INTERRUPTS/ DMA REQUESTS	CLKRUN#	ACTION
0	X	X	None
1	NO CHANGE	X	None
	CHANGE/ASSERTION (**Note 8.43**)	0	None
		1	Assert CLKRUN# (**Note 8.44**)

Note 8.43 "Change/Assertion" means either-edge change on any internal IRQs routed to the SIRQ block or assertion of an internal DMA request by a device in SIO10N268. The "assertion" detection logic runs asynchronously to the PCI Clock and regardless of the Serial IRQ mode; i.e., "continuous" or "quiet".

Note 8.44 The CLKRUN# signal is '1' for at least two consecutive clocks before SIO10N268 asserts ('0') it.

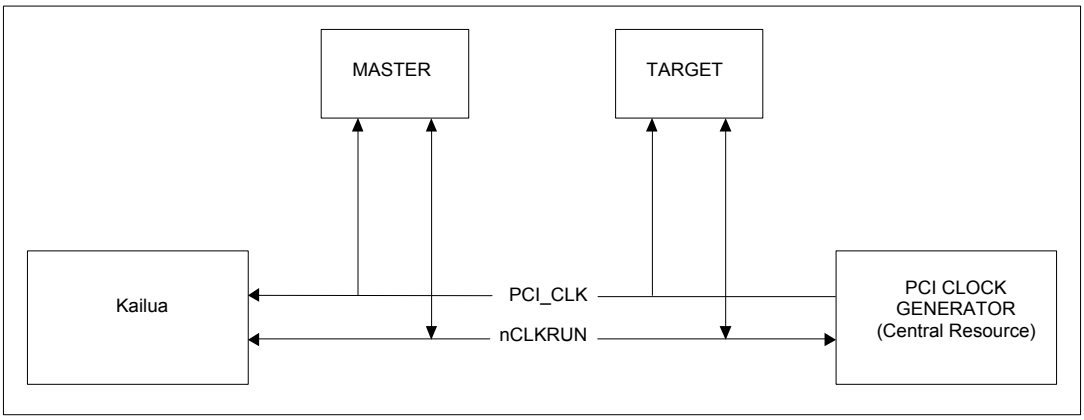


Figure 8.9 - CLKRUN# System Implementation Example

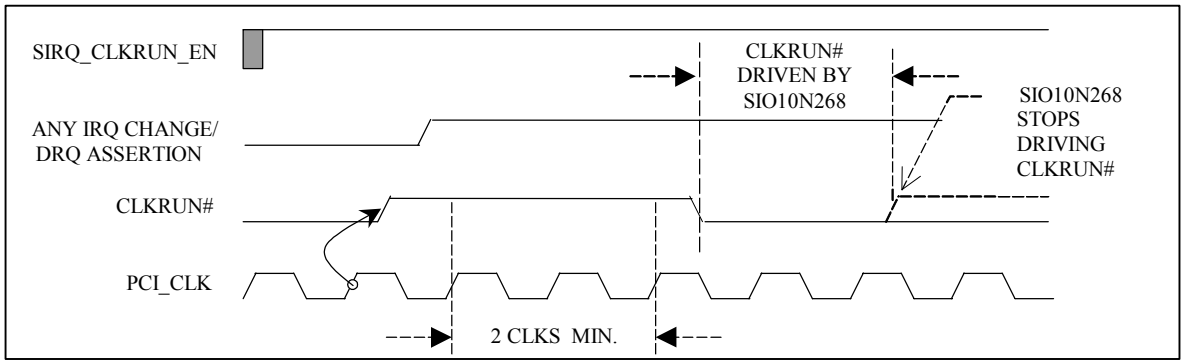


Figure 8.10 - Clock Start Illustration

Note 8.45 The signal "ANY IRQ CHANGE/DRQ ASSERTION" is the same as "CHANGE/ASSERTION" in Table 8.54.

Note 8.46 The SIO10N268 continually monitors the state of CLKRUN# to maintain the PCI Clock until an active "ANY IRQ CHANGE/DRQ ASSERTION" condition has been transferred to the host in a SER_IRQ/DMA cycle. For example, if "ANY IRQ CHANGE/DRQ ASSERTION" is asserted before CLKRUN# is de-asserted (not shown in Figure 8.10), the SIO10N268 must assert CLKRUN# as needed until the SER_IRQ/DMA cycle has completed.

8.16 General Purpose I/O

The SIO10N268 provides a set of flexible Input/Output control functions to the system designer through the 33 independently programmable General Purpose I/O pins (GPIO). The GPIO pins can perform basic I/O and many of them can be individually enabled to generate an SMI and a PME.

8.16.1 GPIO Pins

The following pins include GPIO functionality as defined in the table below.

Table 8.55 - GPIO Pin Functionality

PIN	NAME	POWER WELL	DEFAULT ON VTR POR	DEFAULT ON VCC POR	GPIO PME/SMI FUNCTION
2	GP11/DRVDEN1/FDC_PP	VCC (**Note 8.47**)	GPIO Input	Programmable	PME/SMI
20	GP23/LED2/IRQIN2	VTR (**Note 8.47**)	GPIO Input	Programmable	PME/SMI
34	GP30 /nRI3	VCC (**Note 8.47**, **Note 8.48**)	GPIO Input	Programmable	PME
35	GP31/nDCD3	VCC (**Note 8.47**)	GPIO Input	Programmable	PME
36	GP32/nRXD3	VCC (**Note 8.47**)	GPIO Input	Programmable	PME
37	GP33/nTXD3	VCC (**Note 8.47**)	GPIO Input	Programmable	PME
38	GP34/nDSR3	VCC (**Note 8.47**)	GPIO Input	Programmable	PME
39	GP35/nRTS3	VCC (**Note 8.47**)	GPIO Input	Programmable	PME

PIN	NAME	POWER WELL	DEFAULT ON VTR POR	DEFAULT ON VCC POR	GPIO PME/SMI FUNCTION
40	GP36/nCTS3	VCC (**Note 8.47**)	GPIO Input	Programmable	PME
41	GP37/nDTR3	VCC (**Note 8.47**)	GPIO Input	Programmable	PME
42	GP40/nRI4	VCC (**Note 8.48**)	GPIO Input	Programmable	PME
43	GP41/nDCD4	VCC	GPIO Input	Programmable	-
44	GP42/nRXD4	VCC	GPIO Input	Programmable	-
45	GP43/nTXD4	VCC	GPIO Input	Programmable	-
46	GP44/nDSR4	VCC	GPIO Input	Programmable	-
47	GP45/nRTS4	VCC	GPIO Input	Programmable	-
48	GP46/nCTS4	VCC	GPIO Input	Programmable	-
50	GP47/nDTR4	VCC	GPIO Input	Programmable	-
51	GP12/IO_SMI#	VCC (**Note 8.47**)	GPIO Input	Programmable	IO_SMI#/ PME/SMI
53	GP13/IRQIN1/LED1	VCC (**Note 8.47**)	GPIO Input	Programmable	PME/SMI
55	XA20/GP16	VCC (**Note 8.47**)	X-Bus Address bit[20] Output	Programmable	PME/SMI
56	XA19/GP17	VCC (**Note 8.47**)	X-Bus Address bit[19] Output	Programmable	PME/SMI
60	GP20/IRRX2/IRQIN3	VCC (**Note 8.47**)	GPIO Input	Programmable	PME
61	GP21/IRTX2/WDT	VCC (**Note 8.47**)	GPIO Input	Programmable	PME
62	GP22/IRMODE/IRRX3/nXCS2	VCC (**Note 8.47**)	GPIO Input	Programmable	PME
90	GP50/nRI2	VCC (**Note 8.48**)	GPIO Input	Programmable	PME
91	GP51/nDCD2	VCC	GPIO Input	Programmable	-
92	GP52/RXD2/IRRX	VCC	GPIO Input	Programmable	-
93	GP53/TXD2/IRTX	VCC	GPIO Input	Programmable	-
94	GP54/nDSR2	VCC	GPIO Input	Programmable	-
95	GP55/nRTS2	VCC	GPIO Input	Programmable	-
96	GP56/nCTS2	VCC	GPIO Input	Programmable	-
97	GP57/nDTR2 /MEMEN	VCC	GPIO Input	Programmable	-

Note 8.47 These pins have input buffers into the wakeup logic that are powered by VTR.

Note 8.48 This pin has an input buffer into the wakeup logic that are powered by VTR to support the nRI function.

8.16.2 Description

Each GPIO port has a 1-bit data register. GPIOs are controlled by GPIO control registers located in the Configuration section. The data register for each GPIO port is represented as a bit in one of the 8-bit GPIO DATA Registers, GP1 to GP5. The bits in these registers reflect the value of the associated GPIO pin as follows. Pin is an input: The bit is the value of the GPIO pin. Pin is an output: The value written to the bit goes to the GPIO pin. Latched on read and write. The GPIO data registers are located in the Runtime Register block; see the Runtime Registers section. The GPIO ports with their alternate functions and configuration state register addresses are listed in Table 8.56.

Table 8.56 – General Purpose I/O Port Assignments

PIN NO. /QFP	DEFAULT FUNCTION	ALT. FUNC. 1	ALT. FUNC. 2	ALT. FUNC. 3	DATA REGISTER (Note 8.49)	DATA REGISTER BIT NO.	REGISTER OFFSET (HEX)
N/A	Reserved				GP1	0	0C
2	GPIO	DRVDEN1	FDC_PP			1	
51	GPIO	IO_SMI#				2	
53	GPIO	IRQIN1	nLED1			3	
N/A	Reserved					4	
N/A	Reserved					5	
55	XA20	GPIO				6	
56	XA19	GPIO				7	
60	GPIO	IRRX2	IRQIN3		GP2	0	0D
61	GPIO	IRTX2	WDT			1	
62	GPIO	IRMODE	IRRX3	nXCS2		2	
20	GPIO	nLED2	IRQIN2			3	
N/A	Reserved					4	
N/A	Reserved					5	
N/A	Reserved					6	
N/A	Reserved					7	
34	GPIO	nRI3			GP3	0	0E
35	GPIO	nDCD3				1	
36	GPIO	nRXD3				2	
37	GPIO	nTXD3				3	
38	GPIO	nDSR3				4	
39	GPIO	nRTS3				5	
40	GPIO	nCTS3				6	
41	GPIO	nDTR3				7	
42	GPIO	nRI4			GP4	0	0F
43	GPIO	nDCD4				1	
44	GPIO	nRXD4				2	
45	GPIO	nTXD4				3	
46	GPIO	nDSR4				4	
47	GPIO	nRTS4				5	
48	GPIO	nCTS4				6	
50	GPIO	nDTR4				7	
90	GPIO	nRI5			GP5	0	0F
91	GPIO	nDCD5				1	
92	GPIO	nRXD5				2	
93	GPIO	nTXD5				3	
94	GPIO	nDSR5				4	
95	GPIO	nRTS5				5	
96	GPIO	nCTS5				6	
97	GPIO	nDTR5				7	

Note 8.49 The GPIO Data Registers are located at the offset shown from the RUNTIME REGISTERS BLOCK address.

8.16.3 GPIO Control

Each GPIO port has an 8-bit control register that controls the behavior of the pin. These registers are defined in the Configuration section of this specification.

Each GPIO port may be configured as either an input or an output. If the pin is configured as an output, it can be programmed as open-drain or push-pull. Inputs and outputs can be configured as non-inverting or inverting. GPIO Direction Registers determine the port direction, GPIO Polarity Registers determine the signal polarity, and GPIO Output Type Register determines the output driver type select. The GPIO Output Type Registers (CR39, CR40, CR41) apply to certain GPIOs (GP11-GP13, GP16-GP17, GP20, GP21, GP23, and GP50-GP57). The GPIO Direction, Polarity and Output Type Registers control the GPIO pin when the pin is configured for the GPIO function and when the pin is configured for the alternate function for all pins.

The basic GPIO configuration options are summarized in Table 8.57.

Table 8.57 - GPIO Configuration Summary

SELECTED FUNCTION	DIRECTION BIT	POLARITY BIT	DESCRIPTION
	B0	B1	
GPIO	0	0	Pin is a non-inverted output.
	0	1	Pin is an inverted output.
	1	0	Pin is a non-inverted input.
	1	1	Pin is an inverted input.

8.16.4 GPIO Operation

The operation of the GPIO ports is illustrated in Figure 8.11.

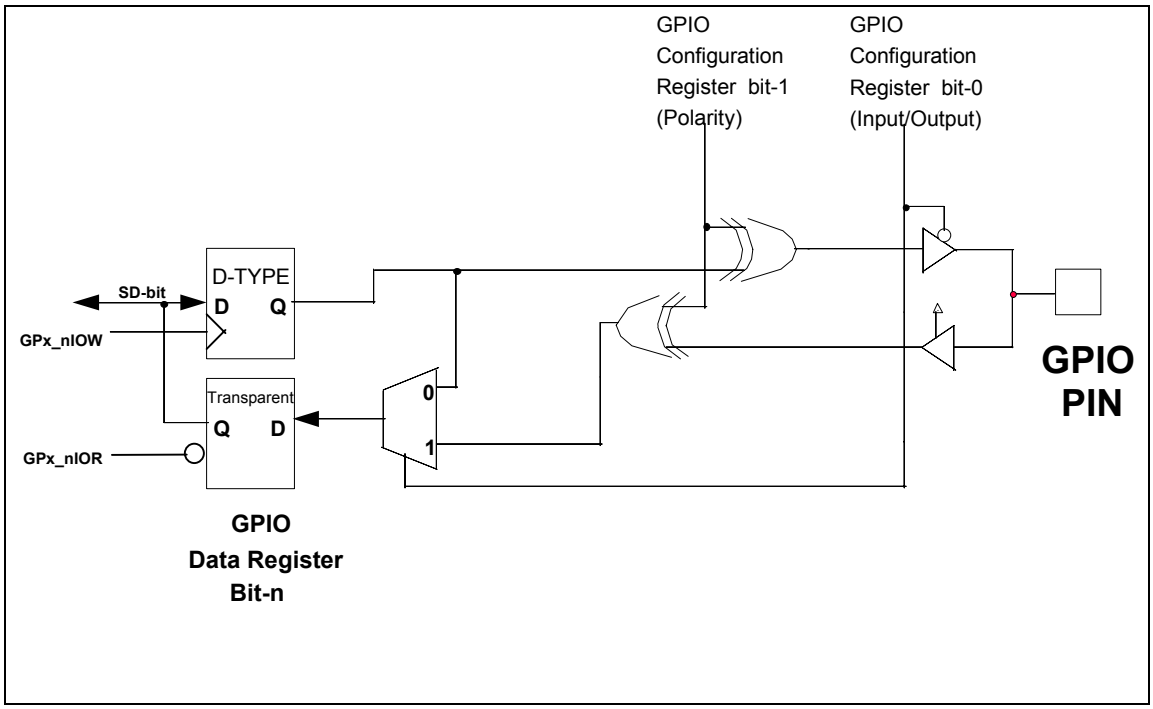


Figure 8.11 - GPIO Function

NOTE: Figure 8.11 is for illustration purposes only and in not intended to suggest specific implementation details.

When a GPIO port is programmed as an input, reading it through the GPIO data register latches either the inverted or non-inverted logic value present at the GPIO pin. Writing to a GPIO port that is programmed as an input has no effect (Table 8.58).

When a GPIO port is programmed as an output, the logic value or the inverted logic value that has been written into the GPIO data register is output to the GPIO pin. Reading from a GPIO port that is programmed as an output returns the last value written to the data register (Table 8.58).

Table 8.58 - GPIO Read/Write Behavior

HOST OPERATION	GPIO INPUT PORT	GPIO OUTPUT PORT
READ	LATCHED VALUE OF GPIO PIN	LAST WRITE TO GPIO DATA REGISTER
WRITE	NO EFFECT	BIT PLACED IN GPIO DATA REGISTER

The SIO10N268 provides 20 GPIOs that can directly generate a PME. See the table in the next section. The GPIO Polarity Registers in the Configuration section select the edge on these GPIO pins that will set the associated status bit in the PME_STS1 – PME_STS4 registers. The default is the low-to-high edge. If the corresponding enable bit in the PME_EN1 – PME_EN4 registers and the PME_EN bit in the PME_EN register is set, a PME will be generated. These registers are located in the Runtime Registers Block, which is located at the address contained in the configuration registers CR30. The PME status bits for the GPIOs are cleared on a write of '1'. In addition, the SIO10N268 provides 6 GPIOs that can directly generate an SMI. See the table in the next section.

8.16.5 GPIO, PME and SMI Functionality

The following GPIOs are dedicated wakeup GPIOs with a status and enable bit in the PME status and enable registers:

- GP11-GP13
- GP16-GP17
- GP20-GP23
- GP30-GP37
- GP40
- GP50

This following is the list of PME status and enable registers for their corresponding GPIOs:

- PME_STS1 and PME_EN1 for GP11-GP13 and GP16-GP17
- PME_STS2 and PME_EN2 for GP20-GP23 and GP50
- PME_STS3 and PME_EN3 for GP30-GP37
- PME_STS4 and PME_EN4 for GP30 and GP40

The following GPIOs can directly generate an SMI and have a status and enable bit in the SMI status and enable registers.

- GP11-GP13
- GP16-GP17
- GP23

The following SMI status and enable registers for these GPIOs:

- SMI_STS1 and SMI_EN1 for GP11-GP13 and GP16-GP17
- SMI_STS2 and SMI_EN2 for GP23

Table 8.59 - PME and SMI Functionality for each GPIO

GPIO	PME	SMI	OUTPUT BUFFER POWER	NOTES
GP11	Yes	Yes	VCC	
GP12	Yes	Yes/IO_SMI#	VCC	**Note 8.50**
GP13	Yes	Yes	VCC	
GP16-GP17	Yes	Yes	VCC	
GP20-GP22	Yes	No	VCC	
GP23	Yes	Yes	VTR	
GP30-GP37	Yes	No	VCC	
GP40	Yes	No	VCC	
GP41-GP47	No	No	VCC	**Note 8.51**
GP50	Yes	No	VCC	
GP51-GP57	No	No	VCC	**Note 8.51**

Note 8.50 Since GP12 can be used to generate an SMI and as the IO_SMI# output, do not enable GP12 to generate an SMI (by setting bit 2 of the SMI Enable Register 1) if the IO_SMI# function is selected on the GP12 pin. Use GP12 to generate an SMI event only if the SMI output is enabled on the Serial IRQ stream.

Note 8.51 GP41-GP47 and GP51-GP57 should not be connected to any VTR powered external circuitry. These pins are not used for wakeup.

8.17 System Management Interrupt (SMI)

The SIO10N268 implements a “group” IO_SMI# output pin. The System Management Interrupt is a non-maskable interrupt with the highest priority level used for OS transparent power management. The nSMI group interrupt output consists of the enabled interrupts from Super I/O Device Interrupts (Parallel Port, Serial Ports 1, 2, 3, and 4, and FDC) and many of the GPIOs pins. The GP12/IO_SMI# pin, when selected for the IO_SMI# function, can be programmed to be active high or active low via bit[2] in the GPIO Polarity Register 1 (CR32). The IO_SMI# pin function defaults to active low. The output buffer type of the pin can be programmed to be open-drain or push-pull via GPIO Output Type Register 1 (CR39).

The interrupts are enabled onto the group nSMI output via the SMI Enable Registers 1, 2, and 3. The nSMI output is then enabled onto the IO_SMI# output pin via bit[7] in the SMI Enable Register 2. The SMI output can also be enabled onto the serial IRQ stream (IRQ2) via Bit[6] in the SMI Enable Register 2.

8.17.1 SMI Registers

There are six SMI Registers located in the Runtime Register block. They are SMI_EN1, SMI_EN2, SMI_EN3, SMI_STS1, SMI_STS2, and SMI_STS3. The SMI event bits for the GPIOs events are located in the SMI status and Enable registers 1 and 2. The polarity of the edge used to set the status bit and generate an SMI is controlled by the GPIO Polarity Registers located in the Configuration section. For non-inverted polarity (default) the status bit is set on the low-to-high edge. Status bits for the GPIOs are cleared on a write of ‘1’.

The SMI logic for the GPIO events is implemented such that the output of the status bit for each event is combined with the corresponding enable bit in order to generate an SMI.

The SMI event bits for the super I/O devices are located in the SMI status and enable registers 2 and 3. All of these status bits are cleared at the source; these status bits are not cleared by a write of ‘1’. The SMI logic for these events is implemented such that each event is directly combined with the corresponding enable bit in order to generate an SMI.

See Chapter 9 Runtime Registers for the definition of the SMI status and enable registers.

8.18 PME Support

The SIO10N268 offers support for Power Management Events (PMEs), also referred to as System Control Interrupt (SCI) events in an ACPI system. A power management event is indicated to the chipset via the assertion of the IO_PME# signal. In the SIO10N268, the IO_PME# is asserted by active transitions on the ring indicator inputs nRI1, nRI2, nRI3, and nRI4, Watchdog Timer Event (WDT), and programmable edges on GPIO pins. The nIO_PME pin can be programmed to be active high or active low via bit 5 in the GPIO Polarity Register 2 (CR34). The nIO_PME pin function defaults to active low, open-drain output. The output buffer type of the pin can be programmed to be open-drain or push-pull via bit 7 in the GPIO Output Type Register 2 (CR40). This pin is powered by VTR. See the Configuration section for description on these registers.

PME functionality is controlled by the PME status and enable registers in the runtime registers block, which is located at the address programmed in register 0x30 in the Configuration section. The PME Enable bit, PME_EN, globally controls PME Wake-up events. When PME_EN is inactive, the IO_PME# signal can not be asserted. When PME_EN is asserted, any wake source whose individual PME Wake Enable register bit is asserted can cause IO_PME# to become asserted.

The PME Status register indicates that an enabled wake source has occurred and if the PME_EN bit is set, asserted the IO_PME# signal. The PME Status bit is asserted by active transitions of PME wake sources. PME_STS will become asserted independent of the state of the global PME enable, PME_EN.

The following pertains to the PME status bits for each event:

- The output of the status bit for each event is combined with the corresponding enable bit to set the PME status bit.
- The status bit for any pending events must be cleared in order to clear the PME_STS bit. Status bits are cleared on a write of '1'.

For the GPIO events, the polarity of the edge used to set the status bit and generate a PME is controlled by the GPIO Polarity Registers in the Configuration section. For non-inverted polarity (default) the status bit is set on the low-to-high edge. Status bits are cleared on a write of '1'.

In the SIO10N268 the IO_PME# pin can be programmed to be an open drain, active low, driver. The SIO10N268 IO_PME# pin is fully isolated from other external devices that might pull the IO_PME# signal low; i.e., the IO_PME# signal is capable of being driven high externally by another active device or pullup even when the SIO10N268 VCC is grounded, providing VTR power is active.

8.18.1 PME Registers

There are eight PME Registers located in the Runtime Register block. They are PME_EN1, PME_EN2, PME_EN3, PME_EN4, PME_STS1, PME_STS2, PME_STS3, and PME_STS4. These registers are located in system I/O space at an offset from Runtime Registers Block, the address programmed at register 0x30 in the Configuration section.

The following registers are for GPIO PME events:

- PME Wake Status 1 (PME_STS1), PME Wake Enable 1 (PME_EN1)
- PME Wake Status 2 (PME_STS2), PME Wake Enable 2 (PME_EN2)
- PME Wake Status 3 (PME_STS3), PME Wake Enable 3 (PME_EN3)
- PME Wake Status 4 (PME_STS4), PME Wake Enable 4 (PME_EN4)

See PME register description in Chapter 9 Runtime Registers.

Chapter 9 Runtime Registers

9.1 Runtime Registers Block Summary

The runtime registers are located at the address programmed in the Runtime Register Block Base Address configuration register located in CR30. The part performs 16-bit address qualification on the Runtime Register Base Address (bits[11:0] are decoded and bits[15:12] must be zero). The runtime register block may be located within the range 0x0100-0x0FFF on 16-byte boundaries. Decodes are disabled if the Runtime Register Base Address is located below 0x100. These registers are powered by VTR.

Table 9.1 - Runtime Register Block Summary

REGISTER OFFSET (hex)	TYPE	Hard RESET (Note 9.3)	VCC POR	VTR POR	REGISTER
00	R/W	-	-	0x00	PME_STS
01	R/W	-	-	0x00	PME_EN
02	R/W	-	-	0x00	PME_STS1
03	R/W	-	-	0x00	PME_STS2
04	R/W	-	-	0x00	PME_STS3
05	R/W	-	-	0x00	PME_EN1
06	R/W	-	-	0x00	PME_EN2
07	R/W	-	-	0x00	PME_EN3
08	R/W	-	-	0x00	SMI_STS1
09	R/W	**Note 9.1**	**Note 9.1**	0x01 **Note 9.1**	SMI_STS2
0A	R/W	-	-	0x00	SMI_EN1
0B	R/W	-	-	0x00	SMI_EN2
0C	R/W	-	-	0x00	GP1
0D	R/W	-	-	0x00	GP2
0E	R/W	-	-	0x00	GP3
0F	R/W	-	-	0x00	GP4
10	R/W	-	-	0x00	GP5
11	R/W	0x00	0x00	0x00	WDT_TIME_OUT
12	R/W	0x00	0x00	0x00	WDT_VAL
13	R/W	0x00	0x00	0x00	WDT_CFG
14	R/W **Note 9.2**	0x00	0x00	0x00	WDT_CTRL
15	R/W	-	-	0x00	LED1
16	R/W	-	-	0x00	LED2
17	R	-	-	0x00	Reserved
18	R/W	-	-	0x00	SMI_STS3
19	R/W	-	-	0x00	SMI_EN3
1A	R/W	-	-	0x00	PME_STS4
1B	R/W	-	-	0x00	PME_EN4

NOTE: Reserved bits return 0 on read.

Note 9.1 The parallel port interrupt defaults to 1 when the parallel port power bit is cleared. When the parallel port is activated, PINT follows the nACK input.

Note 9.2 This register contains some bits that are read or write only.

Note 9.3 Hard Reset = PCI_RESET# OR RESET_DRV.

9.2 Runtime Registers Block Description

Table 9.2 - Runtime Registers Block Description

NAME/DEFAULT	REGISTER OFFSET	DESCRIPTION
PME_STS Default = 0x00 on VTR POR	00 (R/W)	Bit[0] PME_Status = 0 (default) = 1 Set when SIO10N268 would normally assert the IO_PME# signal, independent of the state of the PME_En bit. Bit[7:1] Reserved PME_Status is not affected by Vcc POR, SOFT RESET or HARD RESET. Writing a “1” to PME_Status will clear it and cause the SIO10N268 to stop asserting IO_PME#, in enabled. Writing a “0” to PME_Status has no effect.
PME_EN Default = 0x00 on VTR POR	01 (R/W)	Bit[0] PME_En = 0 IO_PME# signal assertion is disabled (default) = 1 Enables SIO10N268 to assert IO_PME# signal Bit[7:1] Reserved PME_En is not affected by Vcc POR, SOFT RESET or HARD RESET
PME_STS1 Default = 0x00 on VTR POR	02 (R/W)	PME Wake Status Register 1 This register indicates the state of the individual PME wake sources, independent of the individual source enables or the PME_En bit. If the wake source has asserted a wake event, the associated PME Wake Status bit will be a “1”. Bit[0] Reserved Bit[1] GP11 Bit[2] GP12 Bit[3] GP13 Bit[4] Reserved Bit[5] Reserved Bit[6] GP16 Bit[7] GP17 The PME Wake Status register is not affected by Vcc POR, SOFT RESET or HARD RESET. Writing a “1” to Bit[7:0] will clear it. Writing a “0” to any bit in PME Wake Status Register has no effect. Note: Status bits are set by an event on the pin regardless of the Alternate Function selected.

NAME/DEFAULT	REGISTER OFFSET	DESCRIPTION
PME_STS2 Default = 0x00 on VTR POR	03 (R/W)	PME Wake Status Register 2 This register indicates the state of the individual PME wake sources, independent of the individual source enables or the PME_En bit. If the wake source has asserted a wake event, the associated PME Wake Status bit will be a “1”. Bit[0] nRI1 Bit[1] nRI2/GP50 Bit[2] GP20 Bit[3] GP21 Bit[4] GP22 Bit[5] GP23 Bit[6] Reserved Bit[7] WDT Writing a “1” to Bit[7:0] will clear it. Writing a “0” to any bit in PME Wake Status Register has no effect. Note: Status bits are set by an event on the pin regardless of the Alternate Function selected.
PME_STS3 Default = 0x00 on VTR POR	04 (R/W)	PME Wake Status Register 3 This register indicates the state of the individual PME wake sources, independent of the individual source enables or the PME_En bit. If the wake source has asserted a wake event, the associated PME Wake Status bit will be a “1”. Bit[0] GP30/nRI3 Bit[1] GP31 Bit[2] GP32 Bit[3] GP33 Bit[4] GP34 Bit[5] GP35 Bit[6] GP36 Bit[7] GP37 The PME Wake Status register is not affected by Vcc POR, SOFT RESET or HARD RESET. Writing a “1” to Bit[7:0] will clear it. Writing a “0” to any bit in PME Wake Status Register has no effect. Note: Status bits are set by an event on the pin regardless of the Alternate Function selected.

NAME/DEFAULT	REGISTER OFFSET	DESCRIPTION
PME_EN1 Default = 0x00 on VTR POR	05 (R/W)	PME Wake Enable Register 1 This register is used to enable individual SIO10N268 PME wake sources onto the IO_PME# wake bus. When the PME Wake Enable register bit for a wake source is active (“1”), if the source asserts a wake event so that the associated status bit is “1” and the PME_En bit is “1”, the source will assert the IO_PME# signal. When the PME Wake Enable register bit for a wake source is inactive (“0”), the PME Wake Status register will indicate the state of the wake source but will not assert the IO_PME# signal. Bit[0] Reserved Bit[1] GP11 Bit[2] GP12 Bit[3] GP13 Bit[4] Reserved Bit[5] Reserved Bit[6] GP16 Bit[7] GP17 The PME Wake Enable register is not affected by Vcc POR, SOFT RESET or HARD RESET.
PME_EN2 Default = 0x00 on VTR POR	06 (R/W)	PME Wake Enable Register 2 This register is used to enable individual SIO10N268 PME wake sources onto the IO_PME# wake bus. When the PME Wake Enable register bit for a wake source is active (“1”), if the source asserts a wake event so that the associated status bit is “1” and the PME_En bit is “1”, the source will assert the IO_PME# signal. When the PME Wake Enable register bit for a wake source is inactive (“0”), the PME Wake Status register will indicate the state of the wake source but will not assert the IO_PME# signal. Bit[0] nRI1 Bit[1] nRI2/GP50 Bit[2] GP20 Bit[3] GP21 Bit[4] GP22 Bit[5] GP23 Bit[6] Reserved Bit[7] WDT

NAME/DEFAULT	REGISTER OFFSET	DESCRIPTION
PME_EN3 Default = 0x00 on VTR POR	07 (R/W)	PME Wake Enable Register 3 This register is used to enable individual SIO10N268 PME wake sources onto the IO_PME# wake bus. When the PME Wake Enable register bit for a wake source is active (“1”), if the source asserts a wake event so that the associated status bit is “1” and the PME_En bit is “1”, the source will assert the IO_PME# signal. When the PME Wake Enable register bit for a wake source is inactive (“0”), the PME Wake Status register will indicate the state of the wake source but will not assert the IO_PME# signal. Bit[0] GP30/nRI3 Bit[1] GP31 Bit[2] GP32 Bit[3] GP33 Bit[4] GP34 Bit[5] GP35 Bit[6] GP36 Bit[7] GP37 The PME Wake Enable register is not affected by Vcc POR, SOFT RESET or HARD RESET.
SMI_STS1 Default = 0x00 on VTR POR	08 (R/W)	SMI Status Register 1 This register is used to read the status of the SMI inputs. The following bits are cleared on a write of ‘1’. Bit[0] Reserved Bit[1] GP11 Bit[2] GP12 Bit[3] GP13 Bit[4] Reserved Bit[5] Reserved Bit[6] GP16 Bit[7] GP17
SMI_STS2 Default = 0x01 on VTR POR Bit 0 is set to ‘1’ on VCC POR, VTR POR and HARD RESET	09 (R/W)	SMI Status Register 2 This register is used to read the status of the SMI inputs. The bits[3:0] must be cleared at their source. Bits[5:4] are cleared on a write of ‘1’. Bit[0] PINT. The parallel port interrupt defaults to ‘1’ when the parallel port activate bit is cleared. When the parallel port is activated, PINT follows the nACK input. Bit[1] U2INT Bit[2] U1INT Bit[3] FINT Bit[4] GP23 Bit[7:5] Reserved

NAME/DEFAULT	REGISTER OFFSET	DESCRIPTION
SMI_EN1 Default = 0x00 on VTR POR	0A (R/W)	SMI Enable Register 1 This register is used to enable the different interrupt sources onto the internal group nSMI signal. 1=Enable 0=Disable Bit[0] Reserved Bit[1] GP11 Bit[2] GP12 Bit[3] GP13 Bit[4] Reserved Bit[5] Reserved Bit[6] GP16 Bit[7] GP17
SMI_EN2 Default = 0x00 on VTR POR	0B (R/W)	SMI Enable Register 2 This register is used to enable the different interrupt sources onto the internal group nSMI signal, and the internal group nSMI signal onto the IO_SMI# GPI/O pin or the serial IRQ stream on IRQ2. 1=Enable 0=Disable Bit[0] EN_PINT Bit[1] EN_U2INT Bit[2] EN_U1INT Bit[3] EN_FINT Bit[4] GP23 Bit[5] Reserved Bit[6] EN_SMI_S (Enable group nSMI signal onto serial IRQ2) Bit[7] EN_SMI (Enable group nSMI signal onto IO_SMI# pin)
GP1 Default = 0x00 on VTR POR	0C R/W	General Purpose I/O Data Register 1 Bit[0]Reserved Bit[1]GP11 Bit[2]GP12 Bit[3]GP13 Bit[4]Reserved Bit[5]Reserved Bit[6]GP16 Bit[7]GP17
GP2 Default = 0x00 on VTR POR	0D R/W	General Purpose I/O Data Register 2 Bit[0]GP20 Bit[1]GP21 Bit[2]GP22 Bit[3]GP23 Bit[7:4]Reserved

NAME/DEFAULT	REGISTER OFFSET	DESCRIPTION
GP3 Default = 0x00 on VTR POR	0E R/W	General Purpose I/O Data Register 3 Bit[0]GP30 Bit[1]GP31 Bit[2]GP32 Bit[3]GP33 Bit[4]GP34 Bit[5]GP35 Bit[6]GP36 Bit[7]GP37
GP4 Default = 0x00 on VTR POR	0F R/W	General Purpose I/O Data Register 4 Bit[0]GP40 Bit[1]GP41 Bit[2]GP42 Bit[3]GP43 Bit[4]GP44 Bit[5]GP45 Bit[6]GP46 Bit[7]GP47
GP5 Default = 0x00 on VTR POR	10 R/W	General Purpose I/O Data Register 5 Bit[0]GP50 Bit[1]GP51 Bit[2]GP52 Bit[3]GP53 Bit[4]GP54 Bit[5]GP55 Bit[6]GP56 Bit[7]GP57
WDT_TIME_OUT Default = 0x00 on VCC POR, VTR POR, and Hard Reset	11 (R/W)	Watchdog Timeout Bits[6:0] Reserved Bit[7] WDT Time-out Value Units Select = 0 Minutes (default) = 1 Seconds
WDT_VAL Default = 0x00 on VCC POR, VTR POR, and Hard Reset	12 (R/W)	Watchdog Timer Time-out Value Binary coded, units = minutes (default) or seconds, selectable via Bit[7] of WDT_TIME_OUT register (0x52). 0x00 Time out disabled 0x01 Time-out = 1 minute (second) ..... 0xFF Time-out = 255 minutes (seconds)

NAME/DEFAULT	REGISTER OFFSET	DESCRIPTION
WDT_CFG Default = 0x00 on VCC POR, VTR POR, and Hard Reset	13 (R/W)	Watchdog timer Configuration Bit[3:0] Reserved Bits[7:4] WDT Interrupt Mapping 1111 = IRQ15 ..... 0011 = IRQ3 0010 = Invalid 0001 = IRQ1 0000 = Disable
WDT_CTRL Default = 0x00 on VCC POR, VTR POR, and Hard Reset	14 (R/W) Bit[2] is Write-Only	Watchdog timer Control Bit[0] Watchdog Status Bit, R/W (Note) =1 WD timeout occurred =0 WD timer counting Bit[1] Reserved Bit[2] Force Timeout, W =1 Forces WD timeout event; this bit is self-clearing Bit[3] Reserved Bit[7:4] Reserved. Set to 0 Note: If WDT is disabled (i.e., WDT_VAL register is 00h) bit[0] is forced to '0'
LED1 Default = 0x00 on VTR POR	15 (R/W)	Bit[1:0] LED1 Control 00=off 01=Blink at 1Hz rate with a 50% duty cycle (0.5 sec on, 0.5 sec off) 10=Blink at ½ HZ rate with a 25% duty cycle (0.5 sec on, 1.5 sec off) 11=on Bits[7:2] Reserved
LED2 Default = 0x00 on VTR POR	16 (R/W)	Bit[1:0] LED2 Control 00=off 01=Blink at 1Hz rate with a 50% duty cycle (0.5 sec on, 0.5 sec off) 10=Blink at ½ Hz rate with a 25% duty cycle (0.5 sec on, 1.5 sec off) 11=on Bits[7:2] Reserved
Reserved	17	Reads return 0.
SMI_STS3 Default = 0x00 on VTR POR	18 (R/W)	SMI Status Register 3 This register is used to read the status of the SMI inputs. Bit[0] is cleared on a write of '1'. Bit[0] WDT Bit[1] U3INT Bit[2] U4INT Bit[7:3] Reserved

NAME/DEFAULT	REGISTER OFFSET	DESCRIPTION
SMI_EN3 Default = 0x00 on VTR POR	19 (R/W)	SMI Enable Register 3 This register is used to enable the different interrupt sources onto the internal group nSMI signal. 1=Enable 0=Disable Bit[0] EN_WDT Bit[1] EN_U3INT Bit[2] EN_U4INT Bit[7:3] Reserved
PME_STS4 Default = 0x00 on VTR POR	1A (R/W)	PME Wake Status Register 4 This register indicates the state of the individual PME wake sources, independent of the individual source enables or the PME_En bit. If the wake source has asserted a wake event, the associated PME Wake Status bit will be a “1”. Bit[0] nRI3/GP30 Bit[1] nRI4/GP40 Bit[2] Reserved Bit[3] Reserved Bit[4] Reserved Bit[5] Reserved Bit[6] Reserved Bit[7] Reserved Writing a “1” to Bit[1:0] will clear it. Writing a “0” to any bit in PME Wake Status Register has no effect. Note: Status bits are set by an event on the pin regardless of the Alternate Function selected.
PME_EN4 Default = 0x00 on VTR POR	1B (R/W)	PME Wake Enable Register 4 This register is used to enable individual SIO10N268 PME wake sources onto the IO_PME# wake bus. When the PME Wake Enable register bit for a wake source is active (“1”), if the source asserts a wake event so that the associated status bit is “1” and the PME_En bit is “1”, the source will assert the IO_PME# signal. When the PME Wake Enable register bit for a wake source is inactive (“0”), the PME Wake Status register will indicate the state of the wake source but will not assert the IO_PME# signal. Bit[0] nRI3/GP30 Bit[1] nRI4/GP40 Bit[2] Reserved Bit[3] Reserved Bit[4] Reserved Bit[5] Reserved Bit[6] Reserved Bit[7] Reserved

NOTE: Reserved bits return 0 on read.

Chapter 10 Configuration

The configuration of the SIO10N268 is programmed through hardware selectable Configuration Access Ports that appear when the chip is placed into the configuration state. The SIO10N268 logical device blocks, if enabled, will operate normally in the configuration state.

10.1 Configuration Access Ports

The Configuration Access Ports are the CONFIG PORT, the INDEX PORT, and the DATA PORT (Table 10.1). The base address of these registers is controlled by the nRTS1/SYSOPT pin and by the Configuration Port Base Address registers CR12 and CR13. To determine the configuration base address at power-up, the state of the nRTS1/SYSOPT pin is latched by the falling edge of a hardware reset. If the latched state is a 0, the base address of the Configuration Access Ports is located at address 0x02E; if the latched state is a 1, the base address is located at address 0x04E. The base address is relocatable via CR12 and CR13.

Table 10.1 - Configuration Access Ports

PORT NAME	SYSOPT = 0	SYSOPT = 1	TYPE
CONFIG PORT	0x02E	0x04E	WRITE
INDEX PORT	0x02E	0x04E	READ/WRITE (**Note 10.1**, **Note 10.2**)
DATA PORT	INDEX PORT + 1		READ/WRITE (**Note 10.1**)

Note 10.1 The INDEX and DATA ports are active only when the SIO10N268 is in the configuration state.

Note 10.2 The INDEX PORT is only readable in the configuration state.

10.2 Configuration State

The configuration registers are used to select programmable chip options. The SIO10N268 operates in two possible states: the run state and the configuration state. After power up by default the chip is in the run state. To program the configuration registers, the configuration state must be explicitly enabled. Programming the configuration registers typically follows this sequence:

1) Enter the Configuration State,
2) Program the Configuration Register(s),
3) Exit the Configuration State.

10.2.1 Entering the Configuration State

To enter the configuration state write the Configuration Access Key to the CONFIG PORT. The Configuration Access Key is one byte of 55H data. The SIO10N268 will automatically activate the Configuration Access Ports following this procedure.

10.2.2 Configuration Register Programming

The SIO10N268 contains configuration registers CR00-CR54. After the SIO10N268 enters the configuration state, configuration registers can be programmed by first writing the register index number (00 - 54H) to the Configuration Select Register (CSR) through the INDEX PORT and then writing or

reading the configuration register contents through the DATA PORT. Configuration register access remains enabled until the configuration state is explicitly exited.

10.2.3 Exiting the Configuration State

To exit the configuration state, write one byte of AAH data to the CONFIG PORT. The SIO10N268 will automatically deactivate the Configuration Access Ports following this procedure, at which point configuration register access cannot occur until the configuration state is explicitly re-enabled.

10.2.3.1 Programming Example

The following is a configuration register programming example written in Intel 8086 assembly language.

```
;-----------------------------.
; ENTER CONFIGURATION STATE  |
;-----------------------------'
MOV   DX,02EH            ;SYSOPT = 0
MOV   AX,055H
OUT   DX,AL
;-----------------------------.
; CONFIGURE REGISTER CR0-CRx |
;-----------------------------'
MOV   DX,02EH
MOV   AL,00H
OUT   DX,AL              ;Point to CR0
MOV   DX,02FH
MOV   AL,3FH
OUT   DX,AL              ;Update CR0
;
MOV   DX,02EH
MOV   AL,01H
OUT   DX,AL              ;Point to CR1
MOV   DX,02FH
MOV   AL,9FH
OUT   DX,AL              ;Update CR1
;
; Repeat for all CRx registers
;
;-----------------------------.
; EXIT CONFIGURATION STATE   |
;-----------------------------'
MOV   DX,02EH
MOV   AX,AAH
OUT   DX,AL
```

10.2.3.2 Configuration Select Register (CSR)

The Configuration Select Register can only be accessed when the SIO10N268 is in the configuration state. The CSR is located at the INDEX PORT address and must be initialized with configuration register index before the register can be accessed using the DATA PORT.

10.3 Configuration Registers Summary

The configuration registers are set to their default values at power up (Table 10.2) and are RESET as indicated in Table 10.2 and the register descriptions that follow.

Table 10.2 – Configuration Registers Summary

REGISTER INDEX	TYPE	Hard RESET (Note 10.4)	VCC POR	VTR POR	REGISTER
CR00	R/W	Bit[3] = 0	0x20	-	FDC Power/Valid Config Cycle
CR01	R/W	bit[7]=1 Bit[2]=0	0x98	-	PP Power/Mode/CR Lock
CR02	R/W	0x00	0x00	-	UART Power
CR03	R/W	-	0x70	-	FDC Miscellaneous
CR04	R/W	-	0x00	-	PP and UART Miscellaneous
CR05	R/W	-	0x00	-	FDC Setup
CR06	R/W	-	0xFF	-	Drive Type ID
CR07	R/W	bit[7:2]=0	0x00	-	Auto Power Mgt/Boot Drive Select
CR08	R	-	0x00	-	Reserved
CR09	R/W	-	0x00	-	Test 4
CR0A	R/W	bit[7:6]=0	0x00	-	ECP FIFO Threshold/IR MUX
CR0B	R/W	-	0x00	-	Drive Rate
CR0C	R/W	0x02	0x02	-	UART Mode
CR0D	R	-	0x5B	-	Device ID
CR0E	R	-	Revision	-	Revision ID
CR0F	R/W	-	0x00	-	Test 1
CR10	R/W	-	0x00	-	Test 2
CR11	R/W	-	0x00	-	Test 3
CR12	R/W	SYSOPT=0:0x2E SYSOPT=1:0x4E		-	Configuration Base Address 0
CR13	R/W	SYSOPT=0:0x00 SYSOPT=1:0x00		-	Configuration Base Address 1
CR14	R	-	-	-	DSR Shadow
CR15	R	-	-	-	UART1 FCR Shadow
CR16	R	-	-	-	UART2 FCR Shadow
CR17	R/W	0x03	0x03	-	Force FDD Status Change
CR18	R/W	bit[7:6]=0	0x00	-	UART 3,4 Miscellaneous
CR19	R	-	-	-	UART3 FCR Shadow
CR1A	R	-	-	-	UART4 FCR Shadow
CR1B	R/W	-	0x00	-	UART3 Base Address

REGISTER INDEX	TYPE	Hard RESET (Note 10.4)	VCC POR	VTR POR	REGISTER
CR1C	R/W	-	0x00	-	UART4 Base Address
CR1D	R/W	-	0x00	-	UART 3,4 IRQ Select
CR1E	R/W	-	-	0x00	Clock/AEN Control Register
CR1F	R/W	-	0x00	-	Drive Type
CR20	R/W	-	0x3C	-	FDC Base Address
CR21	R/W	-	0x00	-	FDC on PP/EPP Timeout Select
CR22	R/W	0x00	0x00	-	ECP Software Select
CR23	R/W	-	0x00	-	Parallel Port Base Address
CR24	R/W	-	0x00	-	UART1 Base Address
CR25	R/W	-	0x00	-	UART2 Base Address
CR26	R/W	-	0xFF	-	FDC and PP DMA Select
CR27	R/W	-	0x00	-	FDC and PP IRQ Select
CR28	R/W	-	0x00	-	UART IRQ Select
CR29	R/W	-	0x80	-	IRQIN1/HPMODE/SIRQ_CLKRUN_En
CR2A	R/W	-	0x00	-	IRQIN2/IRQIN3
CR2B	R/W	-	0x00	-	SCE (FIR) Base Address
CR2C	R/W	-	0x0F	-	SCE (FIR) DMA Select
CR2D	R/W	-	0x03	-	IR Half Duplex Timeout
CR2E	R/W	-	0x00	-	Software Select A
CR2F	R/W	-	0x00	-	Software Select B
CR30	R/W	-	0x00	-	Runtime Register Block Address
CR31	R/W	-	-	0x00	GPIO Direction Register 1
CR32	R/W	-	-	0x00	GPIO Polarity Register 1
CR33	R/W	-	-	0x00	GPIO Direction Register 2
CR34	R/W	-	-	0x00	GPIO Polarity Register 2
CR35	R/W	-	-	0x00	GPIO Direction Register 3
CR36	R/W	-	-	0x00	GPIO Polarity Register 3
CR37	R/W	-	-	0x00	GPIO Direction Register 4
CR38	R/W	-	-	0x00	GPIO Polarity Register 4
CR39	R/W	-	-	0x00	GPIO Output Type Register 1
CR3A	R/W	-	0x00	-	Test 5
CR3B	R	-	0x00	-	Reserved
CR3C	R	-	0x00	-	Reserved
CR3D	R	-	0x00	-	Reserved
CR3E	R	-	0x00	-	Reserved
CR3F	R	-	0x00	-	Reserved
CR40	R/W	-	-	0x80	GPIO/MISC Output Type Register 2
CR41	R/W	-	-	0x00	GPIO Output Type Register 5
CR42	R/W	-	-	0x00	GPIO Direction Register 5
CR43	R/W	-	-	0x00	GPIO Polarity Register 5
CR44	R/W	-	-	0x00	GPIO Alternate Function Select Register 1
CR45	R/W	bit[7:4]= 0101	bit[7:4]= 0101	0x50	GPIO Alternate Function Select Register 2

REGISTER INDEX	TYPE	Hard RESET (Note 10.4)	VCC POR	VTR POR	REGISTER
CR46	R/W	-	-	0x00	GPIO Alternate Function Select Register 3
CR47	R/W	-	0x00	-	Reserved
CR48	R/W	-	-	0x00	GPIO Alternate Function Select Register 5
CR49	R/W	-	-	0x00	GPIO Alternate Function Select Register 6
CR4A	R/W	-	-	0x00	GPIO Alternate Function Select Register 7
CR4B	R/W	-	-	0x00	GPIO Alternate Function Select Register 8
CR4C	R/W	-	-	0x00	GPIO Alternate Function Select Register 9
CR4D	R/W	-	-	0x00	GPIO Alternate Function Select Register 10
CR4E	R/W (**Note 10.3**)	0x00	0x00	-	X-Bus Base I/O Address for Chip Select 1 - High Byte
CR4F	R/W (**Note 10.3**)	0x01	0x01	-	X-Bus Base I/O Address for Chip Select 1 - Low Byte
CR50	R/W (**Note 10.3**)	0x00	0x00	-	X-Bus Base I/O Address for Chip Select 2 - High Byte
CR51	R/W (**Note 10.3**)	0x01	0x01	-	X-Bus Base I/O Address for Chip Select 2 - Low Byte
CR52	R/W	0x00	0x00	-	X-Bus I/O Select
CR53	R/W (**Note 10.3**)	0x8C	0x8C	-	X-Bus Chip Select 0
CR54	R/W	0XX00000b (**Note 10.5**)	0XX00000b (**Note 10.5**)	-	FWH ID SELECT

NOTE: Reserved registers are read-only, reads return 0.

Note 10.3 These registers are read-only if the write protect bit is set.

Note 10.4 Hard Reset = PCI_RESET# OR RESET_DRV

Note 10.5 X=Strap Options

10.4 Configuration Registers Description

10.4.1 CR00

CR00 can only be accessed in the configuration state and after the CSR has been initialized to 00H.

Table 10.3 - CR00

FDC POWER/VALID CONFIGURATION CYCLE		
TYPE: R/W		**DEFAULT:** 0x20 on VCC POR Bit[3] = 0 on a Hard Reset
BIT NO.	**BIT NAME**	**DESCRIPTION**
0-2	Reserved	Read Only. A read returns 0
3	FDC Power (**Note 10.6**)	A high level on this bit, supplies power to the FDC. A low level on this bit puts the FDC in low power mode (default).
4,5,6	Reserved	Read only. A read returns bit 5 as a 1 and bits 4 and 6 as a 0.
7	Valid	A high level on this software controlled bit can be used to indicate that a valid configuration cycle has occurred. The control software must take care to set this bit at the appropriate times. Set to zero after power up. This bit has no effect on any other hardware in the chip.

Note 10.6 Power Down bits disable the respective logical device and associated pins, however the power down bit does not disable the selected address range for the logical device. To disable the host address registers the logical device's base address must be set below 100h. Devices that are powered down but still reside at a valid I/O base address will participate in Plug-and-Play range checking.

10.4.2 CR01

CR01 can only be accessed in the configuration state and after the CSR has been initialized to 01H.

Table 10.4 – CR01

PP POWER/MODE/CR LOCK		
TYPE: R/W		**DEFAULT:** 0x98 on VCC POR; Bit[7] = 1 and Bit[2]=0 on HARD RESET
BIT NO.	**BIT NAME**	**DESCRIPTION**
0,1	Reserved	Read Only. A read returns "0".
2	Parallel Port Power (**Note 10.7**, **Note 10.8**)	A high level on this bit, supplies power to the Parallel Port. A low level on this bit puts the Parallel Port in low power mode (Default).
3	Parallel Port Mode	Parallel Port Mode. A high level on this bit, sets the Parallel Port for Printer Mode (Default). A low level on this bit enables the Extended Parallel port modes. Refer to Bits 0 and 1 of CR4
4	Reserved	Read Only. A read returns "1".
5,6	Reserved	Read Only. A read returns "0".
7	Lock CRx	A high level on this bit enables the reading and writing of CR00 – CR39 (Default). A low level on this bit disables the reading and writing of CR00 – CR39. Note: once the Lock CRx bit is set to "0", this bit can only be set to "1" by a hard reset or power-up reset.

Note 10.7 Power Down bits disable the respective logical device and associated pins, however the power down bit does not disable the selected address range for the logical device. To disable the host address registers the logical device's base address must be set below 100h. Devices that are powered down but still reside at a valid I/O base address will participate in Plug-and-Play range checking.

Note 10.8 On a VCC POR and a Hard Reset the Parallel Port defaults to powered off. When the Parallel Port Power bit is cleared the parallel port interupt (PINT) located in the SMI_STS2 register at offset 0x09 is set to '1'.

10.4.3 CR02

CR02 can only be accessed in the configuration state and after the CSR has been initialized to 02H.

Table 10.5 – CR02

UART Power		
TYPE: R/W		**DEFAULT:** 0x00 on VCC POR and Hard Reset
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	Reserved	Read Only. A read returns "0".
1	UART3 Power (**Note 10.9**, **Note 10.10**)	A high level on this bit, allows normal operation of the Primary Serial Port. A low level on this bit places the Primary Serial Port into Power Down Mode (Default).
2	UART4 Power (**Note 10.9**, **Note 10.10**)	A high level on this bit, allows normal operation of the Primary Serial Port. A low level on this bit places the Primary Serial Port into Power Down Mode (Default).
3	UART1 Power (**Note 10.9**)	A high level on this bit, allows normal operation of the Primary Serial Port. A low level on this bit places the Primary Serial Port into Power Down Mode (Default).
4-6	Reserved	Read Only. A read returns "0".
7	UART2 Power (**Note 10.9**, **Note 10.10**)	A high level on this bit, allows normal operation of the Secondary Serial Port, including the SCE/FIR block. A low level on this bit places the Secondary Serial Port including the SCE/FIR block into Power Down Mode (Default).

Note 10.9 Power Down bits disable the respective logical device and associated pins, however the power down bit does not disable the selected address range for the logical device. To disable the host address registers the logical device's base address must be set below 100h. Devices that are powered down but still reside at a valid I/O base address will participate in Plug-and-Play range checking.

Note 10.10 The UART pins must be configured for their alternate function prior to enabling the UART power bits. In addition, the IRCC should be configured for the appropriate mode of operation before the UART2 Power bit is set. This is to ensure the state of the transmit and receive pins are in their inactive state for the external device attached and for the internal block that has been enabled, respectively. The registers used to configure the IRCC block are IR Output Mux bits located in the ECP FIFO Threshold/IR MUX located at CR0A and the UART Mode register located at CR0C. These functions may also be configured directly in the SCE registers located in the IR block. A description of these register may be found in the SMSC Infrared Communication Controller (IRCC) specification.

10.4.4 CR03

CR03 can only be accessed in the configuration state and after the CSR has been initialized to 03H.

Table 10.6 - CR03

FDC MISCELLANEOUS		
TYPE: R/W		**DEFAULT:** 0x70 on VCC POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	Reserved	Read Only. A read returns 0.
1	Enhance Floppy Mode 2	Bit 1 — Floppy Mode (Note) 0 — NORMAL Floppy Mode (Default) 1 — Enhanced Floppy Mode 2 (OS2) Note: Refer to the description of the TAPE DRIVE REGISTER (TDR) for more information on these modes.
2,3	Reserved	Read Only. A read returns 0.
4	DRVDEN1	Bit 4 — Pin DRVDEN1 Output (Note) 0 — Output Programmed DRVDEN1 Value 1 — Force DRVDEN1 Output High (default) Note: See **Note 10.15** in section 10.4.6 CR05.
5	MFM	IDENT is used in conjunction with MFM to define the FDC interface mode.
6	IDENT	IDENT / MFM / MODE 1 / 1 / AT Mode (Default) 1 / 0 / Reserved 0 / 1 / PS/2 0 / 0 / Model 30
7	Reserved	Read Only. A read returns 0.

10.4.5 CR04

CR04 can only be accessed in the configuration state and after the CSR has been initialized to 04H.

Table 10.7 - CR04

PP AND UART MISCELLANEOUS				
TYPE: R/W			**DEFAULT:** 0x00 on VCC POR	
BIT NO.	**BIT NAME**	**DESCRIPTION**		
1,0	Parallel Port Extended Modes	Bit 1	Bit 0	If CR1 bit 3 is a low level then:
		0	0	Standard and Bi-directional Modes (SPP) (default)
		0	1	EPP Mode and SPP
		1	0	ECP Mode (**Note 10.12**)
		1	1	ECP Mode & EPP Mode (**Note 10.11**, **Note 10.12**)

PP AND UART MISCELLANEOUS		
TYPE: R/W		**DEFAULT:** 0x00 on VCC POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
2,3	Parallel Port FDC	Refer to Parallel Port Floppy Disk Controller description. Bit 3 Bit 2 0 0 Normal 0 1 PPFD1 1 0 PPFD2 1 1 Reserved
4	MIDI 1 (**Note 10.13**)	Serial Clock Select Port 1: A low level on this bit disables MIDI support (default). A high level on this bit enables MIDI support.
5	MIDI 2 ((**Note 10.13**)	Serial Clock Select Port 2: A low level on this bit disables MIDI support (default). A high level on this bit enables MIDI support.
6	EPP Type	0 = EPP 1.9 (default) 1 = EPP 1.7
7	Reserved	Reserved - Read as 0.

Note 10.11 In this mode, EPP can be selected through the ecr register of ECP as mode 100.

Note 10.12 In these modes, 2 drives can be supported directly, 3 or 4 drives must use external 4 drive support. SPP can be selected through the ecr register of ECP as mode 000.

Note 10.13 MIDI Support: The Musical Instrumental Digital Interface (MIDI) operates at 31.25Kbaud (+/-1%).

10.4.6 CR05

CR05 can only be accessed in the configuration state and after the CSR has been initialized to 05H.

Table 10.8 – CR05

FLOPPY DISK SETUP REGISTER				
TYPE: R/W		**DEFAULT:** 0x00 on VCC POR		
BIT NO.	**BIT NAME**	**DESCRIPTION**		
0 (**Note 10.14**)	FDC Output Type Control (R/W)	0 = FDC Outputs are open drain (default). 1 = FDC Outputs are push-pull.		
1 (**Note 10.14**, **Note 10.15**)	FDC Output Control (R/W)	0 = FDC Outputs Active (default). 1 = FDC Outputs Tri-State.		
2	FDC DMA Mode	0 = Burst mode is enabled for the FDC FIFO execution phase data transfers (default). 1 = Non-Burst mode enabled.		
4,3	DenSel	**BIT 4**	**BIT 3**	**DENSEL OUTPUT**
		0	0	Normal (default)
		0	1	Reserved
		1	0	1
		1	1	0
5	Swap Drives 0,1	0= do not swap (default). 1= swap drives and motor select 0 and 1 of the FDC on the parallel port.		
6,7	Reserved	Read Only. A read returns 0.		

Note 10.14 Bits CR05[1:0] do not affect the Parallel Port FDC.

Note 10.15 In the SIO10N268, the behavior of the DRVDEN1 Control CR03.4 depends upon the FDC Output Control CR05.1 (Table 10.9). If the FDC Output Control is active DRVDEN1 will behave as follows if CR03.4 is 0 the DRVDEN1 output pin assumes the value of the DRVDEN1 function, if CR03.4 is 1 the DRVDEN1 output pin stays high. If the FDC Output Control is inactive the DRVDEN1 Control will have no affect on the DRVDEN1 output pin.

Table 10.9 - DRVDEN1 Control

FDC OUTPUT CONTROL (CR05.1)	DRVDEN1 CONTROL (CR03.4)	DRVDEN1 (PIN 2)	DESCRIPTION
0	0	1/0	Normal DRVDEN1 function
0	1	1	DRVDEN1 forced high
1	X	Tristate	All FDD output pins are tristated

10.4.7 CR06

CR06 can only be accessed in the configuration state and after the CSR has been initialized to 06H. CR06 holds the floppy disk drive type IDs for up to four floppy disk drives (see Table 8.11 - Drive Type ID in 8.7 Floppy Disk Controller).

Table 10.10 - CR06

DRIVE TYPE ID REGISTER		
TYPE: R/W		**DEFAULT:** 0xFF on VCC POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	ID00	Floppy Disk Drive 0 type ID 00.
1	ID01	Floppy Disk Drive 0 type ID 01.
2	ID10	Floppy Disk Drive 1 type ID 10.
3	ID11	Floppy Disk Drive 1 type ID 11.
4	ID20	Floppy Disk Drive 2 type ID 00.
5	ID21	Floppy Disk Drive 2 type ID 01.
6	ID30	Floppy Disk Drive 3 type ID 10.
7	ID31	Floppy Disk Drive 4 type ID 11.

10.4.8 CR07

CR07 can only be accessed in the configuration state and after the CSR has been initialized to 07H. CR07 controls auto power management and the floppy boot drive.

Table 10.11 – CR07

AUTO POWER MANAGEMENT AND BOOT DRIVE SELECT		
TYPE: R/W		**DEFAULT:** 0x00 on VCC POR; Bits[7:2] = 000000b on HARD RESET
BIT NO.	**BIT NAME**	**DESCRIPTION**
0,1	Floppy Boot	This bit is used to define the boot floppy. 0 = Drive A (default) 1 = Drive B
2	UART 3 Enable	This bit controls the AUTOPOWER DOWN feature of the UART3. The function is: 0 = Auto powerdown disabled (default) 1 = Auto powerdown enabled This bit is reset to the default state by VCC POR or a hardware reset.
3	UART 4 Enable	This bit controls the AUTOPOWER DOWN feature of the UART4. The function is: 0 = Auto powerdown disabled (default) 1 = Auto powerdown enabled This bit is reset to the default state by VCC POR or a hardware reset.
4	Parallel Port Enable	This bit controls the AUTOPOWER DOWN feature of the Parallel Port. The function is: 0 = Auto powerdown disabled (default) 1 = Auto powerdown enabled This bit is reset to the default state by VCC POR or a hardware reset.
5	UART 2 Enable	This bit controls the AUTOPOWER DOWN feature of the UART2. The function is: 0 = Auto powerdown disabled (default) 1 = Auto powerdown enabled This bit is reset to the default state by VCC POR or a hardware reset.
6	UART 1 Enable	This bit controls the AUTOPOWER DOWN feature of the UART1. The function is: 0 = Auto powerdown disabled (default) 1 = Auto powerdown enabled This bit is reset to the default state by VCC POR or a hardware reset.
7	Floppy Disk Enable	This bit controls the AUTOPOWER DOWN feature of the Floppy Disk. The function is: 0 = Auto powerdown disabled (default) 1 = Auto powerdown enabled (See note in the “FDC Power Management” section) This bit is reset to the default state by VCC POR or a hardware reset.

10.4.9 CR08

Register CR08 is reserved. The default value of this register after power up is 00H.

10.4.10 CR09

CR09 can only be accessed in the configuration state and after the CSR has been initialized to 09H. CR09 is a test control register and all bits must be treated as Reserved.

NOTE: All test modes are reserved for SMSC use. Activating test mode registers may produce undesired results.

Table 10.12 - CR09

TEST 4		
TYPE: R/W		**DEFAULT:** 0x00 on VCC POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	Test 24	RESERVED FOR SMSC USE
1	Test 25	
2	Test 26	
3	Test 27	
4	Test 28	
5	Test 29	
6	Test 30	
7	Test 31	

10.4.11 CR0A

CR0A can only be accessed in the configuration state and after the CSR has been initialized to 0AH. CR0A defines the FIFO threshold for the ECP mode parallel port. Bits [5:4] are Reserved. Reserved bits cannot be written and return 0 when read. Bits [7:6] are the IR OUTPUT MUX bits and are reset to the default state by a POR and a hardware reset.

Table 10.13 - CR0A

ECP FIFO THRESHOLD/IR MUX		
TYPE: R/W		**DEFAULT:** 0x00 on VCC POR; Bits[7:6] = 00 on HARD RESET
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	THR0	ECP FIFO Threshold 0.
1	THR1	ECP FIFO Threshold 1.
2	THR2	ECP FIFO Threshold 2.
3	THR3	ECP FIFO Threshold 3.
4,5	Reserved	Read Only. A read returns 0.

ECP FIFO THRESHOLD/IR MUX				
TYPE: R/W				**DEFAULT:** 0x00 on VCC POR; Bits[7:6] = 00 on HARD RESET
BIT NO.	**BIT NAME**	**DESCRIPTION**		
6,7	IR Output Mux	These bits are used to select IR Output Mux Mode.		
		BIT7	**BIT6**	**MUX MODE**
		0	0	Active device to COM port (Default). That is, depending on the mode of Serial Port 2, use Pins 90-97 for COM signals or use RXD2 and TXD2 (pins 92 and 93) for IR. When Serial Port 2 is inactive (UART2 Power bit = 0), then TXD2 signal is tristate. The IRTX2 signal is low.
		0	1	Active device to IR port. That is, use IRRX2, IRTX2 (pins 60, 61). When Serial Port 2 is inactive (UART2 Power bit = 0), then IRTX2 signal is low. The TXD2 signal is low.
		1	0	Reserved.
		1	1	Outputs Inactive: TXD2/IRTX and IRTX2 are High-Z, regardless of mode of UART2 and state of UART2 powerdown bit.

10.4.12 CR0B

CR0B can only be accessed in the configuration state and after the CSR has been initialized to 0BH. CR0B indicates the Drive Rate table (Table 10.15) used for each drive. Refer to section CR1F for the Drive Type register.

Table 10.14 – CR0B

DRIVE RATE			
TYPE: R/W			**DEFAULT:** 0x00 on VCC POR
BIT NO.	**BIT NAME**	**DESCRIPTION**	
0	DTR0	Floppy Disk Drive 0 Drive Rate Table Bit 0.	
1	DTR1	Floppy Disk Drive 0 Drive Rate Table Bit 1.	
2	DTR0	Floppy Disk Drive 1 Drive Rate Table Bit 0.	
3	DTR1	Floppy Disk Drive 1 Drive Rate Table Bit 1.	
4	DTR0	Floppy Disk Drive 2 Drive Rate Table Bit 0.	
5	DTR1	Floppy Disk Drive 2 Drive Rate Table Bit 1.	
6	DTR0	Floppy Disk Drive 3 Drive Rate Table Bit 0.	
7	DTR1	Floppy Disk Drive 3 Drive Rate Table Bit 1.	

Table 10.15 - Drive Rate Table (Recommended)

DRT1	DRT0	FORMAT
0	0	360K, 1.2M, 720K, 1.44M and 2.88M Vertical Format
0	1	3-Mode Drive
1	0	2 Meg Tape
1	1	Reserved

10.4.13 CR0C

CR0C can only be accessed in the configuration state and after the CSR has been initialized to 0CH. CR0C controls the operating mode of the UART. This register is reset to the default state by a POR or a hardware reset.

Table 10.16 – CR0C

UART MODE		
TYPE: R/W		**DEFAULT:** 0x02 on VCC POR and HARD RESET
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	UART 2 RCV Polarity	0 = RX input active high (default). 1 = RX input active low.
1	UART 2 XMIT Polarity	0 = TX output active high. 1 = TX output active low (default).
2	UART 2 Duplex	This bit is used to define the FULL/HALF DUPLEX operation of UART 2. 1 = Half duplex 0 = Full duplex (default)
3, 4, 5	UART 2 MODE	UART 2 Mode (**Note 10.16**) 5 4 3 0 0 0 Standard COM Functionality (default) 0 0 1 IrDA (HPSIR) 0 1 0 Amplitude Shift Keyed IR 0 1 1 Reserved (**Note 10.17**) 1 x x Reserved (**Note 10.17**)
6	UART 1 Speed	This bit enables the high speed mode of UART 1. 1 = High speed enabled 0 = Standard (default)
7	UART 2 Speed	This bit enables the high speed mode of UART 2. 1 = High speed enabled 0 = Standard (default)

Note 10.16 The UART 2 Mode may be selected by writing bits[5:3] shown or by programming the block control bits located in Register Block One - SCE Configuration Register A of the SCE (FIR) block. See the IrCC Specification dated 5/10/96 for a detailed description of this register and the modes supported.

Note 10.17 Writing these reserved bit combinations will place the IR block into an alternate mode, which is beyond the scope of this specification. Users that require these advanced options should refer to the IrCC Specification dated 5/10/96.

10.4.14 CR0D

CR0D can only be accessed in the configuration state and after the CSR has been initialized to 0DH. This register is read only. CR0D contains the SIO10N268 Device ID. The default value of this register after power up is 5BH on VCC POR.

10.4.15 CR0E

CR0E can only be accessed in the configuration state and after the CSR has been initialized to 0EH. This register is read only. CR0E contains the current SIO10N268 Chip Revision Level starting at 00H.

10.4.16 CR0F

CR0F can only be accessed in the configuration state and after the CSR has been initialized to 0FH. CR0F is a test control register and all bits must be treated as Reserved.

NOTE: All test modes are reserved for SMSC use. Activating test mode registers may produce undesired results.

Table 10.17 - CR0F

TEST 1		
TYPE: R/W		**DEFAULT:** 0x00 on VCC POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	Test 0	RESERVED FOR SMSC USE
1	Test 1	
2	Test 2	
3	Test 3	
4	Test 4	
5	Test 5	
6	Test 6	
7	Test 7	

10.4.17 CR10

CR10 can only be accessed in the configuration state and after the CSR has been initialized to 10H. CR10 is a test control register and all bits must be treated as Reserved. NOTE: All test modes are reserved for SMSC use. Activating test mode registers may produce undesired results.

Table 10.18 – CR10

TEST 2		
TYPE: R/W		**DEFAULT:** 0x00 on VCC POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	Test 8	RESERVED FOR SMSC USE
1	Test 9	
2	Test 10	
3	Test 11	
4	Test 12	
5	Test 13	
6	Test 14	
7	Test 15	

10.4.18 CR11

CR11 can only be accessed in the configuration state and after the CSR has been initialized to 11H. CR11 is a test control register and all bits must be treated as Reserved.

NOTE: All test modes are reserved for SMSC use. Activating test mode registers may produce undesired results.

Table 10.19 - CR11

TEST 3		
TYPE: R/W		**DEFAULT:** 0x00 on VCC POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	Test 16	RESERVED FOR SMSC USE
1	Test 17	
2	Test 18	
3	Test 19	
4	Test 20	
5	Test 21	
6	Test 22	
7	Test 23	

10.4.19 CR12 - CR13

CR12 and CR13 are the SIO10N268 Configuration Ports base address registers (Table 10.20 and Table 10.21). These registers are used to relocate the Configuration Ports base address beyond the power-up defaults determined by the SYSOPT pin programming.

CR12 contains the Configuration Ports base address bits A[7:0]. CR13 contains the Configuration Ports base address bits A[10:8]. The address bits A[15:11] must be '00000' to access the configuration port.

The Configuration Ports base address is relocatable on even-byte boundaries; i.e., A0 = '0'.

At power-up the Configuration Ports base address is determined by the SYSOPT pin programming. To relocate the Configuration Ports base address after power-up, first write the lower address bits of the new base address to CR12 and then write the upper address bits to CR13.

NOTE: Writing CR13 changes the Configuration Ports base address.

Table 10.20 - CR12

CONFIGURATION PORTS BASE ADDRESS BYTE 0 (Note 10.18)		
TYPE: R/W		**DEFAULT:** 0x2E (SYSOPT=0) 0x4E (SYSOPT=1) on VCC POR and HARD RESET
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	Reserved	Read Only. A read returns 0.
1	A1	Configuration Ports Base Address Byte 0 for decoder.
2	A2	
3	A3	
4	A4	
5	A5	
6	A6	
7	A7	

Note 10.18 The Configuration Ports Base Address is relocatable on even-byte boundaries; i.e., A0 = "0".

Table 10.21 - CR13

CONFIGURATION PORTS BASE ADDRESS BYTE 1 (Note 10.19)		
TYPE: R/W		**DEFAULT:** 0x00 (SYSOPT=0) 0x00 (SYSOPT=1) on VCC POR and HARD RESET
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	A8	Configuration Ports Base Address Byte 1 for decoder.
1	A9	
2	A10	
3-7	Reserved	Read Only. A read returns 0.

Note 10.19 Writing CR13 changes the Configuration Ports base address.

10.4.20 CR14

CR14 can only be accessed in the configuration state and after the CSR has been initialized to 14H. CR14 shadows the bits in the write-only FDC run-time DSR register.

Table 10.22 - CR14

DSR SHADOW REGISTER		
TYPE: R		**DEFAULT:** N/A
BIT NO.	**BIT NAME**	**DESCRIPTION**
0,1	Data Rate Select 0-1	These bits the data rate of the floppy controller.
2-4	PRECOMP 0-2	These three bits select the value of write precompensation that will be applied to the WDATA output signal
5	Reserved	Read Only. A read returns 0.
6	PWRDOWN	A logic "1" written to this bit will put the floppy controller into manual low power mode
7	SOFTRESET	A logic "0" written to this bit resets the floppy disk controller. This bit is self clearing.

10.4.21 CR15

CR15 can only be accessed in the configuration state and after the CSR has been initialized to 15H. CR15 shadows the bits in the write-only UART1 run-time FCR register.

Table 10.23 - CR15

UART1 FCR SHADOW REGISTER		
TYPE: R **(Note 10.20)**		**DEFAULT:** N/A
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	FIFO Enable	Setting this bit to a logic "1" enables both the XMIT and RCVR FIFOs
1	RCVR FIFO Reset	Setting this bit to a logic "1" clears all bytes in the RCVR FIFO and resets its counter logic to 0. This bit is self clearing.

UART1 FCR SHADOW REGISTER				
TYPE: R **(Note 10.20)**			**DEFAULT:** N/A	
BIT NO.	**BIT NAME**	**DESCRIPTION**		
2	XMIT FIFO Reset	Setting this bit to a logic "1" clears all bytes in the XMIT FIFO and resets its counter logic to 0. This bit is self-clearing.		
3	DMA Mode Select	Writing to this bit has no effect on the operation of the UART.		
4,5	Reserved	Read Only. A read returns 0.		
6,7	RCVR Trigger	These bits are used to set the trigger level for the RCVR FIFO interrupt.		
		BIT7	**BIT6**	**RCVR FIFO Trigger Level (BYTES)**
		0	0	1
		0	1	4
		1	0	8
		1	1	14

Note 10.20 This is a read only register. Software may set these register bits by writing the UART1 runtime FCR register located at an offset of +2 from the UART1 Base I/O Address. See Table 10.86 - I/O Base Address Configuration Register Description.

10.4.22 CR16

CR16 can only be accessed in the configuration state and after the CSR has been initialized to 16H. CR16 shadows the bits in the write-only UART2 run-time FCR register. See CR15 for register description.

NOTE: This is a read only register. Software may set these register bits by writing the UART2 runtime FCR register located at an offset of +2 from the UART2 Base I/O Address. See Table 10.86 - I/O Base Address Configuration Register Description.

10.4.23 CR17

CR17 can only be accessed in the configuration state and after the CSR has been initialized to 17H. CR17 is the Force FDD Status Change register.

Table 10.24 - CR17

FORCE FDD STATUS CHANGE REGISTER		
TYPE: R/W		**DEFAULT:** 0x03 on VCC POR and Hard Reset
BIT NO.	**BIT NAME**	**DESCRIPTION**
0,1	Force DSKCHG 0-1	Setting either of the Force Disk Change bits active (1) forces the FDD nDSKCHG input active when the appropriate drive has been selected. FORCE DSKCHG1 and FORCE DSKCHG0 can be written to a 1 but are not clearable by software. FORCE DSKCHG1 is cleared on (nSTEP AND nDS1), FORCE DSKCHG0 is cleared on (nSTEP AND nDS0). Note: The DSK CHG bit in the Floppy DIR register, Bit 7 = (nDS0 AND FORCE DSKCHG0) OR (nDS1 AND FORCE DSKCHG1) OR nDSKCHG. Setting either of the Force Disk Change bits active (1) forces the FDD nDSKCHG input active when the appropriate drive has been selected. Bit[0] Force Change for FDC0 0=Inactive 1=Active Bit[1] Force Change for FDC1 0=Inactive 1=Active
2	Force WRTPRT	FORCE WRTPRT asserts the internal nWRTPRT input to the controller when the FORCE WRTPRT bit is active (“1”) and a drive has been selected. The FORCE WRTPRT function applies to the nWRTPRT pin in the FDD Interface as well as the nWRTPRT pin in the Parallel Port FDC.
3-7	Reserved	Read Only. A read returns 0.

NOTE: The controls in the Force FDD Status Change register (CR17) apply to the FDD Interface pins as well as to the Parallel Port FDC.

10.4.24 CR18

CR18 can only be accessed in the configuration state and after the CSR has been initialized to 18H.

Table 10.25 – CR18

UART 3,4 MISCELLANEOUS		
TYPE: R/W		**DEFAULT:** 0x00 on VCC POR, bits[6:7] are reset on Hard Reset
BIT NO.	**BIT NAME**	**DESCRIPTION**
0-3	Reserved	Reserved - Read as 0.
4	MIDI 3 (**Note 10.21**)	Serial Clock Select Port 3: A low level on this bit disables MIDI support (default). A high level on this bit enables MIDI support.
5	MIDI 4 (**Note 10.21**)	Serial Clock Select Port 4: A low level on this bit disables MIDI support (default). A high level on this bit enables MIDI support.
6	UART 3 Speed	This bit enables the high speed mode of UART 3. 1 = High speed enabled 0 = Standard (default)
7	UART 4 Speed	This bit enables the high speed mode of UART 4. 1 = High speed enabled 0 = Standard (default)

Note 10.21 MIDI Support: The Musical Instrumental Digital Interface (MIDI) operates at 31.25Kbaud (+/-1%).

10.4.25 CR19

CR19 can only be accessed in the configuration state and after the CSR has been initialized to 19H. CR19 shadows the bits in the write-only UART3 run-time FCR register.

Table 10.26 - CR19

UART3 FCR SHADOW REGISTER				
TYPE: R **(Note 10.22)**			**DEFAULT:** N/A	
BIT NO.	**BIT NAME**	**DESCRIPTION**		
0	FIFO Enable	Setting this bit to a logic "1" enables both the XMIT and RCVR FIFOs		
1	RCVR FIFO Reset	Setting this bit to a logic "1" clears all bytes in the RCVR FIFO and resets its counter logic to 0. This bit is self clearing.		
2	XMIT FIFO Reset	Setting this bit to a logic "1" clears all bytes in the XMIT FIFO and resets its counter logic to 0. This bit is self-clearing.		
3	DMA Mode Select	Writing to this bit has no effect on the operation of the UART.		
4,5	Reserved	Read Only. A read returns 0.		
6,7	RCVR Trigger	These bits are used to set the trigger level for the RCVR FIFO interrupt.		
		BIT7	**BIT6**	**RCVR FIFO Trigger Level (BYTES)**
		0	0	1
		0	1	4
		1	0	8
		1	1	14

Note 10.22 This is a read only register. Software may set these register bits by writing the UART3 runtime FCR register located at an offset of +2 from the UART3 Base I/O Address. See Table 10.86 - I/O Base Address Configuration Register Description.

10.4.26 CR1A

CR1A can only be accessed in the configuration state and after the CSR has been initialized to 1AH. CR1A shadows the bits in the write-only UART4 run-time FCR register.

Table 10.27 - CR1A

UART4 FCR SHADOW REGISTER			
TYPE: R (Note)		**DEFAULT:** N/A	
BIT NO.	**BIT NAME**	**DESCRIPTION**	
0	FIFO Enable	Setting this bit to a logic "1" enables both the XMIT and RCVR FIFOs	
1	RCVR FIFO Reset	Setting this bit to a logic "1" clears all bytes in the RCVR FIFO and resets its counter logic to 0. This bit is self clearing.	
2	XMIT FIFO Reset	Setting this bit to a logic "1" clears all bytes in the XMIT FIFO and resets its counter logic to 0. This bit is self-clearing.	
3	DMA Mode Select	Writing to this bit has no effect on the operation of the UART.	
4,5	Reserved	Read Only. A read returns 0.	

UART4 FCR SHADOW REGISTER				
TYPE: R (Note)			**DEFAULT:** N/A	
BIT NO.	**BIT NAME**	**DESCRIPTION**		
6,7	RCVR Trigger	These bits are used to set the trigger level for the RCVR FIFO interrupt.		
		BIT7	**BIT6**	**RCVR FIFO Trigger Level (BYTES)**
		0	0	1
		0	1	4
		1	0	8
		1	1	14

Note 10.23 This is a read only register. Software may set these register bits by writing the UART4 runtime FCR register located at an offset of +2 from the UART4 Base I/O Address. See Table 10.86 - I/O Base Address Configuration Register Description.

10.4.27 CR1B

CR1B can only be accessed in the configuration state and after the CSR has been initialized to 1BH. CR1B is used to select the base address of Serial Port 3 (UART3). The serial port can be set to 96 locations on 8-byte boundaries from 100H - 3F8H. To disable Serial Port 3, set ADR9 and ADR8 to zero. Set CR1B.0 to 0 when writing the UART3 Base Address.

Serial Port 3 Address Decoding: address bits A[15:10] must be '000000' to access UART3 registers. A[2:0] are decoded as XXXb.

Table 10.28 - CR1B

UART3 BASE ADDRESS REGISTER			
TYPE: R/W		**DEFAULT:** 0x00 on VCC POR	
BIT NO.	**BIT NAME**	**DESCRIPTION**	
0	Reserved	Read Only. A read returns 0.	
1	ADR3	Serial Port 3 Base Address bits for decoder.	
2	ADR4		
3	ADR5		
4	ADR6		
5	ADR7		
6	ADR8		
7	ADR9		

10.4.28 CR1C

CR1C can only be accessed in the configuration state and after the CSR has been initialized to 1CH. CR1C is used to select the base address of Serial Port 4 (UART4). The serial port can be set to 96 locations on 8-byte boundaries from 100H - 3F8H. To disable Serial Port 4, set ADR9 and ADR8 to zero. Set CR1C.0 to 0 when writing the UART4 Base Address.

Serial Port 4 Address Decoding: address bits A[15:10] must be '000000' to access UART4 registers. A[2:0] are decoded as XXXb.

Table 10.29 - CR1C

UART4 BASE ADDRESS REGISTER		
TYPE: R/W		**DEFAULT:** 0x00 on VCC POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	Reserved	Read Only. A read returns 0.
1	ADR3	Serial Port 4 Base Address bits for decoder.
2	ADR4	
3	ADR5	
4	ADR6	
5	ADR7	
6	ADR8	
7	ADR9	

10.4.29 CR1D

CR1D can only be accessed in the configuration state and after the CSR has been initialized to 1DH. CR1D is used to select the IRQ for Serial Port 3 (bits 7 - 4) and for Serial Port 4 (bits 3 - 0). Refer to the IRQ encoding for CR27. Any unselected IRQ output is in tristate. Shared IRQs are not supported in the SIO10N268.

Table 10.30 - CR1D

UART 3, 4 INTERRUPT SELECTION		
TYPE: R/W		**DEFAULT:** 0x00 on VCC POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0-3	UART4 IRQ Select	These bits are used to select IRQ for Serial Port 4. See IRQ encoding for CR27.
4-7	UART3 IRQ Select	These bits are used to select IRQ for Serial Port 3. See IRQ encoding for CR27.

Table 10.31 - UART Interrupt Operation

UARTX		IRQ
UARTX OUT2 BIT	**UARTX IRQ OUTPUT STATE**	**UARTX IRQ STATE**
0	Z	Z
1	asserted	1
1	de-asserted	0

NOTE: It is the responsibility of the software to ensure that two IRQ's are not set to the same IRQ number. Potential damage to chip may result.

NOTE: Z = Don't Care.

10.4.30 CR1E

CR1E can only be accessed in the Configuration State and after the CSR has been initialized to 1EH.

Table 10.32 - CR1E

CLOCK/AEN CONTROL REGISTER		
TYPE: R/W		**DEFAULT:** 0x00 on VTR POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	CLOCKI32	Bit[0] (CLK32_PRSN) 0=32kHz clock is connected to the CLKI32 pin (default) 1=32kHz clock is not connected to the CLKI32 pin (pin is grounded)
1	AEN Control	AEN Control bit 0=Internal AEN signal should be asserted if the AEN pin is high OR if SA[0:15]=0000h. 1=Internal AEN signal should be asserted only if the AEN pin is high.
2-7	Reserved	Reserved – Read as 0.

10.4.31 CR1F

CR1F can only be accessed in the configuration state and after the CSR has been initialized to 1FH. CR1F indicates the floppy disk Drive Type for each of four floppy disk drives. The floppy disk Drive Type is used to map the three FDC DENSEL, DRATE1 and DRATE0 outputs onto two Super I/O output pins DRVDEN1 and DRVDEN0 (Table 10.34).

Table 10.33 - CR1F

DRIVE TYPE		
TYPE: R/W		**DEFAULT:** 0x00 on VCC POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	DT1	Drive Type Bit 1 for FDD 0.
1	DT0	Drive Type Bit 0 for FDD 0.
2	DT1	Drive Type Bit 1 for FDD 1.
3	DT0	Drive Type Bit 0 for FDD 1.
4	DT1	Drive Type Bit 1 for FDD 2.
5	DT0	Drive Type Bit 0 for FDD 2.
6	DT1	Drive Type Bit 1 for FDD 3.
7	DT0	Drive Type Bit 0 for FDD 3.

Table 10.34 - Drive Type Encoding

DRIVE TYPE		DRVDEN0	DRVDEN1	DRIVE TYPE DESCRIPTION
DT0	DT1			
0	0	DENSEL	DRATE0	4/2/1 MB 3.5” 2/1 MB 5.25” FDDS 2/1.6/1 MB 3.5” (3-MODE)
0	1	DRATE1	DRATE0	
1	0	nDENSEL	DRATE0	PS/2
1	1	DRATE0	DRATE1	

10.4.32 CR20

CR20 can only be accessed in the configuration state and after the CSR has been initialized to 20H. CR20 is used to select the base address of the floppy disk controller (FDC). The FDC base address can be set to 48 locations on 16 byte boundaries from 100H - 3F8H. To disable the FDC set ADR9 and ADR8 to zero. Set CR20.[1:0] to 00b when writing the FDC Base Address.

FDC Address Decoding: address bits A[15:10] must be ‘000000’ to access the FDC registers. A[3:0] are decoded as 0XXXb.

Table 10.35 - CR20

FDC BASE ADDRESS		
TYPE: R/W		**DEFAULT:** 0x3C on VCC POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	Reserved	Read Only. A read returns 0.
1	Reserved	Read Only. A read returns 0.
2	ADR4	FDC Base Address bits for decoder.
3	ADR5	
4	ADR6	
5	ADR7	
6	ADR8	
7	ADR9	

10.4.33 CR21

CR21 can only be accessed in the configuration state and after the CSR has been initialized to 21H. CR21 is the Floppy on Parallel Port Pin register.

Table 10.36 - CR21

FDC ON PP/EPP TIMEOUT SELECT				
TYPE: R/W				**DEFAULT:** 0x00 on VCC POR
BIT NO.	**BIT NAME**	**DESCRIPTION**		
0,1	FDC_PP	**FDC ON PARALLEL PORT PIN**		
		BIT1	**BIT0**	**DESCRIPTION**
		0	0	Bits in PP mode Register control the FDC on the parallel port, the FDC_PP pin function is not used.

		0	1	The FDC_PP pin controls the FDC on the PP as follows: (non-inverted polarity) when the pin is low, the parallel port pins are used for a floppy disk controller: drive 0 is on FDC pins, drive 1 is on parallel port pins.
		1	0	The FDC_PP pin controls the FDC on the PP as follows: (non-inverted polarity) when the pin is low, the parallel port pins are used for a floppy disk controller: drive 0 is on parallel port pins and drive 1 is on parallel port pins.
		1	1	Reserved
2	TIMEOUT_SELECT	This bit selects the means of clearing the TIMEOUT bit in the EPP Status register. If the TIMEOUT_SELECT bit is cleared (‘0’), the TIMEOUT bit is cleared on the trailing edge of the read of the EPP Status Register (default). If the TIMEOUT_SELECT bit is set (‘1’), the TIMEOUT bit is cleared on a write of ‘1’ to the TIMEOUT bit.		
3-7	Reserved	Read Only. A read returns 0.		

10.4.34 CR22

The ECP Software Select register CR22 contains the ECP IRQ Select bits and the ECP DMA Select bits. CR22 is part of the ECP DMA/IRQ Software Indicators described in the ECP cnfgB register. CR22 is read/write.

NOTE: All of the ECP DMA/IRQ Software Indicators, including CR22, are software-only. Writing these bits does not affect the ECP hardware DMA or IRQ channels that are configured in CR26 and CR27.

Table 10.37 - CR22

ECP SOFTWARE SELECT REGISTER		
TYPE: R/W		**DEFAULT:** 0x00 on VCC POR and Hard Reset
BIT NO.	**BIT NAME**	**DESCRIPTION**
2:0	ECP DMA Select	ECP DMA software Indicator
5:3	ECP IRQ Select	ECP IRQ Software Indicator
6,7	Reserved	Read Only. A read returns 0.

10.4.35 CR23

CR23 can only be accessed in the configuration state and after the CSR has been initialized to 23H. CR23 is used to select the base address of the parallel port. If EPP is not enabled, the parallel port can be set to 192 locations on 4-byte boundaries from 100H - 3FCH; if EPP is enabled, the parallel port can be set to 96 locations on 8-byte boundaries from 100H - 3F8H. To disable the parallel port, set ADR9 and ADR8 to zero.

Parallel Port Address Decoding: address bits A[15:10] must be ‘000000’ to access the Parallel Port when in Compatible, Bi-directional, or EPP modes. A10 is active when in ECP mode.

Table 10.38 - CR23

PARALLEL PORT BASE ADDRESS		
TYPE: R/W		**DEFAULT:** 0x00 on VCC POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	ADR2	Parallel Port Base Address bits for decoder.
1	ADR3	

PARALLEL PORT BASE ADDRESS		
TYPE: R/W		**DEFAULT:** 0x00 on VCC POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
2	ADR4	
3	ADR5	
4	ADR6	
5	ADR7	
6	ADR8	
7	ADR9	

Table 10.39 - Parallel Port Addressing Options

EPP ENABLED	ADDRESSING (LOW BITS) DECODE
No	A[1:0] = XXb
Yes	A[2:0] = XXXb

10.4.36 CR24

CR24 can only be accessed in the configuration state and after the CSR has been initialized to 24H. CR24 is used to select the base address of Serial Port 1 (UART1). The serial port can be set to 96 locations on 8-byte boundaries from 100H - 3F8H. To disable Serial Port 1, set ADR9 and ADR8 to zero. Set CR24.0 to 0 when writing the UART1 Base Address.

Serial Port 1 Address Decoding: address bits A[15:10] must be '000000' to access UART1 registers. A[2:0] are decoded as XXXb.

Table 10.40 - CR24

UART1 BASE ADDRESS REGISTER		
TYPE: R/W		**DEFAULT:** 0x00 on VCC POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	Reserved	Read Only. A read returns 0.
1	ADR3	Serial Port 1 Base Address bits for decoder.
2	ADR4	
3	ADR5	
4	ADR6	
5	ADR7	
6	ADR8	
7	ADR9	

10.4.37 CR25

CR25 can only be accessed in the configuration state and after the CSR has been initialized to 25H. CR25 is used to select the base address of Serial Port 2 (UART2). Serial Port 2 can be set to 96 locations on 8-byte boundaries from 100H - 3F8H. To disable Serial Port 2, set ADR9 and ADR8 to zero. Set CR25.0 to 0 when writing the UART2 Base Address.

Serial Port 2 Address Decoding: address bits A[15:10] must be '000000' to access UART2 registers. A[2:0] are decoded as XXXb.

Table 10.41 - CR25

UART2 BASE ADDRESS REGISTER		
TYPE: R/W		**DEFAULT:** 0x00 on VCC POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	Reserved	Read Only. A read returns 0.
1	ADR3	Serial Port 2 Base Address bits for decoder.
2	ADR4	
3	ADR5	
4	ADR6	
5	ADR7	
6	ADR8	
7	ADR9	

10.4.38 CR26

CR26 can only be accessed in the configuration state and after the CSR has been initialized to 26H. CR26 is used to select the DMA for the FDC (Bits 4 - 7) and the Parallel Port (bits 0 - 3). Any unselected DMA Request output (DRQ) is in tristate.

Table 10.42 - CR26

FDC AND PP DMA SELECTION REGISTER		
TYPE: R/W		**DEFAULT:** 0xFF on VCC POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
3:0	PP DMA Select	These bits are used to select DMA for Parallel Port.
7:4	FDC DMA Select	These bits are used to select DMA for Floppy Disk Controller.

Table 10.43 - DMA Selection

BITS[3:0] OR BITS[7:4]	DMA SELECTED
0000	DMA0
0001	DMA1
0010	DMA2 (**Note 10.24**)
0011	DMA3
0100	Reserved
....	…. ….
1110	Reserved
1111	None

Note 10.24 In LPC_MODE the FDC must be assigned to DMA Channel 2.

10.4.39 CR27

CR27 can only be accessed in the configuration state and after the CSR has been initialized to 27H. CR27 is used to select the IRQ for the FDC (Bits 4 - 7) and the Parallel Port (bits 3 - 0). Any unselected IRQ output (registers CR27 - CR29) is in tri-state.

Table 10.44 - CR27

FDC AND PP IRQ SELECTION REGISTER		
TYPE: R/W		**DEFAULT:** 0x00 on VCC POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
3:0	PP IRQ Select	These bits are used to select IRQ for Parallel Port.
7:4	FDC IRQ Select	These bits are used to select IRQ for Floppy Disk Controller.

Table 10.45 – IRQ Encoding

BITS[3:0] OR BITS[7:4]	IRQ SELECTED
0000	NONE
0001	IRQ_1
0010	IRQ_2
0011	IRQ_3
0100	IRQ_4
0101	IRQ_5
0110	IRQ_6
0111	IRQ_7
1000	IRQ_8
1001	IRQ_9
1010	IRQ_10
1011	IRQ_11
1100	IRQ_12
1101	IRQ_13
1110	IRQ_14
1111	IRQ_15

10.4.40 CR28

CR28 can only be accessed in the configuration state and after the CSR has been initialized to 28H. CR28 is used to select the IRQ for Serial Port 1 (bits 7 - 4) and for Serial Port 2 (bits 3 - 0). Refer to the IRQ encoding for CR27 (Table 10.45). Any unselected IRQ output (registers CR27 - CR29) is in tristate. Shared IRQs are not supported in the SIO10N268.

Table 10.46 - CR28

UART INTERRUPT SELECTION		
TYPE: R/W		**DEFAULT:** 0x00 on VCC POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
3:0	UART2 IRQ Select	These bits are used to select IRQ for Serial Port 2. See IRQ encoding for CR27 (Table 10.45 – IRQ Encoding).

7:4	UART1 IRQ Select	These bits are used to select IRQ for Serial Port 1. See IRQ encoding for CR27 (Table 10.45 – IRQ Encoding).

Table 10.47 – UART Interrupt Operation

UARTX		IRQ
UARTX OUT2 BIT	**UARTX IRQ OUTPUT STATE**	**UARTX IRQ STATE**
0	Z	Z
1	asserted	1
1	de-asserted	0

NOTE: It is the responsibility of the software to ensure that two IRQ's are not set to the same IRQ number. Potential damage to chip may result.

NOTE: Z = Don't Care.

10.4.41 CR29

CR29 can only be accessed in the configuration state and after the CSR has been initialized to 29H. CR29 controls the HPMODE bit and is used to select the IRQ mapping (bits 0 - 3) for the IRQIN1 pin. Refer to IRQ encoding for CR27 (Table 10.45). Any unselected IRQ output (registers CR27 - CR29) is in tristate.

Table 10.48 - CR29

IRQIN1/HPMODE/SIRQ_CLKRUN_En			
TYPE: R/W		**DEFAULT:** 0x80 on VCC POR	
BIT NO.	**BIT NAME**	**DESCRIPTION**	
0-3	IRQIN1	Selects the IRQ for IRQIN1. (See Application Note in the "Routable IRQ Inputs" section)	
4	HPMODE	See Figure 8.8 - Infrared Interface Block Diagram	
		0	Select IRMODE (default)
		1	Select IRRX3
5-6	RESERVED	Not Writeable, Reads Return "0"	
7	SIRQ_CLKRUN_EN	Serial IRQ and CLKRUN enable bit. 0 = Disable 1 = Enable (default)	

10.4.42 CR2A

CR2A can only be accessed in the configuration state and after the CSR has been initialized to 2AH. CR2A is used to select the IRQ mapping for the IRQIN2 and IRQIN3 pins. Refer to IRQ encoding for CR27. Any unselected IRQ output (registers CR27 - CR29) is in tristate.

Table 10.49 - CR2A

IRQIN2		
TYPE: R/W		**DEFAULT:** 0x00 on VCC POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0-3	IRQIN2	Selects the IRQ for IRQIN2.
4-7	IRQIN3	Selects the IRQ for IRQIN3.

10.4.43 CR2B

CR2B can only be accessed in the configuration state and after the CSR has been initialized to 2BH. CR2B is used to set the SCE (FIR) base address ADR[10:3]. The SCE base address can be set to 224 locations on 8-byte boundaries from 100H - 7F8H. To disable the SCE, set ADR10, ADR9 and ADR8 to zero.

SCE Address Decoding: address bits A[15:11] must be '00000' to access SCE registers. A[2:0] are decoded as XXXb.

Table 10.50 - CR2B

SCE (FIR) BASE ADDRESS REGISTER		
TYPE: R/W		**DEFAULT:** 0x00 on VCC POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	ADR3	FIR Base Address bits for decoder.
1	ADR4	
2	ADR5	
3	ADR6	
4	ADR7	
5	ADR8	
6	ADR9	
7	ADR10	

10.4.44 CR2C

CR2C can only be accessed in the configuration state and after the CSR has been initialized to 2CH. Bits D[3:0] of this register are used to select the DMA for the SCE (FIR). Bits D[7:4] are Reserved. Reserved bits cannot be written and return 0 when read. Any unselected DMA Request output (DRQ) is in tristate.

Table 10.51 - CR2C

SCE (FIR) DMA SELECT REGISTER						
TYPE: R/W					**DEFAULT:** 0x0F on VCC POR	
BIT NO.	**BIT NAME**	**DESCRIPTION**				
3:0	DMA Select	**BIT3**	**BIT2**	**BIT1**	**BIT0**	**DMA SELECTED**
		0	0	0	0	DMA0
		0	0	0	1	DMA1
		0	0	1	0	DMA2 (**Note 10.25**)
		0	0	1	1	DMA3
		0	1	0	0	RESERVED
		.	.	.	.	.
		.	.	.	.	.
		1	1	1	0	RESERVED
		1	1	1	1	NONE
7:4	Reserved	Read Only. A read returns 0.				

Note 10.25 In LPC_MODE the FDC must be assigned to DMA Channel 2.

10.4.45 CR2D

CR2D can only be accessed in the configuration state and after the CSR has been initialized to 2DH. CR2D is used to set the IR Half Duplex Turnaround Delay Time for the IR port. This value is 0 to 25.5msec in 100µsec increments.

The IRCC v2.0 block includes an 8 bit IR Half Duplex Time-out register in SCE Register Block 5, Address 1 that interacts with configuration register CR2D. These two registers behave like the other IRCC Legacy controls where either source uniformly updates the value of both registers when either register is explicitly written using IOW or following a device-level POR. IRCC software resets do not affect these registers.

The IR Half Duplex Time-out is programmable from 0 to 25.5mS in 100µS increments, as follows:

IR HALF DUPLEX TIME-OUT = (CR2D) x 100µS

Table 10.52 - CR2D

IR HALF DUPLEX TIMEOUT		
TYPE: R/W		**DEFAULT:** 0x03 on VCC POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0-7	IR Half Duplex Time Out	These bits are used to set the IR Half Duplex Turnaround Delay Time for the IR port. This value is 0 to 25.5msec in 100µsec increments.

10.4.46 CR2E

CR2E can only be accessed in the configuration state and after the CSR has been initialized to 2EH. CR2E is directly connected to SCE Register Block Three, Address 0x05 in the IRCC v2.0 block.

Table 10.53 - CR2E

SOFTWARE SELECT A		
TYPE: R/W		**DEFAULT:** 0x00 on VCC POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0-7	Software Select A	These bits are directly connected to SCE Register Block Three, Address 0x05 in the IRCC v2.0 block.

10.4.47 CR2F

CR2F can only be accessed in the configuration state and after the CSR has been initialized to 2FH. CR2F is directly connected to SCE Register Block Three, Address 0x06 in the IRCC v2.0 block.

Table 10.54 - CR2F

SOFTWARE SELECT B		
TYPE: R/W		**DEFAULT:** 0x00 on VCC POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0-7	Software Select B	These bits are directly connected to SCE Register Block Three, Address 0x06 in the IRCC v2.0 block.

10.4.48 CR30

CR30 can only be accessed in the configuration state and after the CSR has been initialized to 30H. CR30 is used to set the Runtime Register Block base address ADR[11:5]. The Runtime Register Block base address can be set to 120 locations on 32-byte boundaries from 100H – FE0H. To disable Runtime Registers Block set the Base Address to a value below 100h (i.e., set ADR11 – ADR8 to zero).

Runtime Register Address Decoding: To access registers located in the Runtime Register block the I/O address bits A[15:12] must be '0000' and the address bits A[11:5] must match the value programmed in the Base Address Register below. I/O address bits A[4:0] are used as the register offset value into the register block. (For example: If A[4:0] = '00000' then the PME_STS register will be accessed).

Table 10.55 - CR30

RUNTIME REGISTERS BLOCK BASE ADDRESS		
TYPE: R/W		**DEFAULT:** 0x00 on VCC POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	Reserved	The bits in this register are used to program the location of the Runtime Register Block Base Address.
1	ADR5	
2	ADR6	
3	ADR7	
4	ADR8	
5	ADR9	
6	ADR10	
7	ADR11	

10.4.49 CR31

CR31 can only be accessed in the configuration state and after the CSR has been initialized to 31H. CR31 is GPIO Direction Register 1 and is used to select the direction of GP11-GP13 and GP16-GP17 pins.

Table 10.56 – CR31

GPIO DIRECTION REGISTER 1		
TYPE: R/W		**DEFAULT:** 0x00 on VTR POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	Reserved	The bits in this register are used to select the direction of the GP11-GP13 and GP16-GP17 pins. 0=Input 1=Output
1	GP11	
2	GP12	
3	GP13	
4	Reserved	
5	Reserved	
6	GP16	
7	GP17	

10.4.50 CR32

CR32 can only be accessed in the configuration state and after the CSR has been initialized to 32H. CR32 is GPIO Polarity Register 1 and is used to select the polarity of GP11-GP13 and GP16-GP17 pins.

Table 10.57 - CR32

GPIO POLARITY REGISTER 1		
TYPE: R/W		**DEFAULT:** 0x00 on VTR POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	Reserved	The bits in this register are used to select the polarity of the GP11-GP13 and GP16-GP17 pins. 0=Non-Inverted 1=Inverted
1	GP11	
2	GP12	
3	GP13	
4	Reserved	
5	Reserved	
6	GP16	
7	GP17	

10.4.51 CR33

CR33 can only be accessed in the configuration state and after the CSR has been initialized to 33H. CR33 is GPIO Direction Register 2. It is used to select the direction of GP20-GP23 pins.

Table 10.58 - CR33

GPIO DIRECTION REGISTER 2		
TYPE: R/W		**DEFAULT:** 0x00 on VTR POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	GP20	These bits are used to select the direction of the GP20-GP23. 0=Input 1=Output
1	GP21	
2	GP22	
3	GP23	
4	Reserved	Read Only. A read returns 0.
5	Reserved	Read Only. A read returns 0.
6	Reserved	Read Only. A read returns 0.
7	Reserved	Read Only. A read returns 0.

10.4.52 CR34

CR35 can only be accessed in the configuration state and after the CSR has been initialized to 34H. CR35 is GPIO Polarity Register 2. It is used to select the polarity of GP20-GP23 and IO_PME pins.

Table 10.59 – CR34

GPIO POLARITY REGISTER 2		
TYPE: R/W		**DEFAULT:** 0x00 on VTR POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	GP20	These bits are used to select the polarity of the GP20-GP23 pins. 0=Non-Inverted 1=Inverted
1	GP21	
2	GP22	
3	GP23	
4	Reserved	Read Only. A read returns 0.

GPIO POLARITY REGISTER 2		
TYPE: R/W		**DEFAULT:** 0x00 on VTR POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
5	IO_PME# Polarity select	This bit is used to select the polarity of the IO_PME# pin. 0=Non-Inverted 1=Inverted Note: configuring this pin function with non-inverted polarity will give an active low output signal. The output type can be either open drain or push-pull. (See CR39).
6	Reserved	Read Only. A read returns 0.
7	Reserved	Read Only. A read returns 0.

10.4.53 CR35

CR35 can only be accessed in the configuration state and after the CSR has been initialized to 35H. CR35 is GPIO Direction Register 3 and is used to select the direction of GP30-GP37 pins.

Table 10.60 - CR35

GPIO DIRECTION REGISTER 3		
TYPE: R/W		**DEFAULT:** 0x00 on VTR POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	GP30	The bits in this register are used to select the direction of the GP30-GP37 pins. 0=Input 1=Output
1	GP31	
2	GP32	
3	GP33	
4	GP34	
5	GP35	
6	GP36	
7	GP37	

10.4.54 CR36

CR36 can only be accessed in the configuration state and after the CSR has been initialized to 36H. CR36 is GPIO Polarity Register 3 and is used to select the polarity of GP30-GP37 pins.

Table 10.61 – CR36

GPIO POLARITY REGISTER 3		
TYPE: R/W		**DEFAULT:** 0x00 on VTR POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	GP30	The bits in this register are used to select the polarity of the GP30-GP37 pins. 0=Non-Inverted 1=Inverted
1	GP31	
2	GP32	
3	GP33	
4	GP34	
5	GP35	
6	GP36	
7	GP37	

10.4.55 CR37

CR37 can only be accessed in the configuration state and after the CSR has been initialized to 37H. CR37 is GPIO Direction Register 4 and is used to select the direction of GP40-GP47 pins.

Table 10.62 – CR37

GPIO DIRECTION REGISTER 4		
TYPE: R/W		**DEFAULT:** 0x00 on VTR POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	GP40	The bits in this register are used to select the direction of the GP40-GP47 pins. 0=Input 1=Output
1	GP41	
2	GP42	
3	GP43	
4	GP44	
5	GP45	
6	GP46	
7	GP47	

10.4.56 CR38

CR38 can only be accessed in the configuration state and after the CSR has been initialized to 38H. CR38 is GPIO Polarity Register 4 and is used to select the polarity of GP40-GP47 pins.

Table 10.63 - CR38

GPIO POLARITY REGISTER 4		
TYPE: R/W		**DEFAULT:** 0x00 on VTR POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	GP40	The bits in this register are used to select the polarity of the GP40-GP47 pins. 0=Non-Inverted 1=Inverted
1	GP41	
2	GP42	
3	GP43	
4	GP44	
5	GP45	
6	GP46	
7	GP47	

10.4.57 CR39

CR39 can only be accessed in the configuration state and after the CSR has been initialized to 39H. CR39 is GPIO Output Register and is used to select the output buffer of GP11-GP13 and GP16-GP17 pins.

Table 10.64 - CR39

GPIO OUTPUT TYPE REGISTER 1		
TYPE: R/W		**DEFAULT:** 0x00 on VTR POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	Reserved	The bits in this register are used to select the output buffer type of the GP11-GP13 and GP16-GP17 pins. 0=Push-pull 1=Open Drain
1	GP11	
2	GP12	
3	GP13	
4	Reserved	
5	Reserved	
6	GP16	
7	GP17	

Note 10.26 When the GP11/DRVDEN1/FDC_PP pin is set for alternate function DRVDEN1 the output type will be determined by bit[0] of CR05.

10.4.58 CR3A

CR3A can only be accessed in the configuration state and after the CSR has been initialized to 3AH. CR3A is a test control register and all bits must be treated as Reserved.

NOTE: All test modes are reserved for SMSC use. Activating test mode registers may produce undesired results.

Table 10.65 - CR3A

TEST 5		
TYPE: R/W		**DEFAULT:** 0x00 on VCC POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	Test 32	RESERVED FOR SMSC USE
1	Test 33	
2	Test 34	
3	Test 35	
4	Test 36	
5	Test 37	
6	Test 38	
7	Test 39	

10.4.59 CR3B – CR3F

CR3A – CR3F registers are reserved. Reserved registers cannot be written and return 0 when read. The default value of these registers after power up is 00H on VCC POR.

10.4.60 CR40

CR40 can only be accessed in the configuration state and after the CSR has been initialized to 40H. CR40 is GPIO Output Register and is used to select the output buffer for the GP20, GP21, GP23, and IO_PME# pins.

Table 10.66 – CR40

GPIO/MISC OUTPUT TYPE REGISTER 2		
TYPE: R/W		**DEFAULT:** 0x80 on VTR POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	GP20	The bits in this register are used to select the output buffer type of the GP20, GP21, GP23, and IO_PME# pins. 0=Push-pull 1=Open Drain
1	GP21	
2	Reserved	
3	GP23	
4	Reserved	
5	Reserved	
6	Reserved	
7	IO_PME#	

10.4.61 CR41

CR41can only be accessed in the configuration state and after the CSR has been initialized to 41H. CR41is GPIO Output Register and is used to select the output buffer of GP50 to GP57 pins.

Table 10.67 - CR41

GPIO OUTPUT TYPE REGISTER 5		
TYPE: R/W		**DEFAULT:** 0x00 on VTR POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	GP50	The bits in this register are used to select the output buffer type of GP50 to GP57 pins. 0=Push-pull 1=Open Drain
1	GP51	
2	GP52	
3	GP53	
4	GP54	
5	GP55	
6	GP56	
7	GP57	

10.4.62 CR42

CR42 can only be accessed in the configuration state and after the CSR has been initialized to 42H. CR42 is GPIO Direction Register 5 and is used to select the direction of GP50-GP57 pins.

Table 10.68 – CR42

GPIO DIRECTION REGISTER 5		
TYPE: R/W		**DEFAULT:** 0x00 on VTR POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	GP50	The bits in this register are used to select the direction of the GP50-GP57 pins. 0=Input 1=Output
1	GP51	
2	GP52	
3	GP53	
4	GP54	
5	GP55	
6	GP56	
7	GP57	

10.4.63 CR43

CR43 can only be accessed in the configuration state and after the CSR has been initialized to 43H. CR43 is GPIO Polarity Register 5 and is used to select the polarity of GP50-GP57 pins.

Table 10.69 - CR43

GPIO POLARITY REGISTER 5		
TYPE: R/W		**DEFAULT:** 0x00 on VTR POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	GP50	The bits in this register are used to select the polarity of the GP50-GP57 pins. 0=Non-Inverted 1=Inverted
1	GP51	
2	GP52	
3	GP53	
4	GP54	
5	GP55	
6	GP56	
7	GP57	

10.4.64 CR44

CR44 can only be accessed in the configuration state and after the CSR has been initialized to 44H. The bits in this register are used to select an alternate function of GP11-GP13 pins.

Table 10.70 - CR44

GPIO ALTERNATE FUNCTION SELECT REGISTER 1		
TYPE: R/W		**DEFAULT:** 0x00 on VTR POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0,1	Reserved	Reads return 0.
2,3	GP11	Alternate Function Select bit[3] bit[2] Function 0 0 GPIO (default) 0 1 DRVDEN1 1 0 FDC_PP (Note) 1 1 Reserved See **Note 10.27** below.
4,5	GP12	Alternate Function Select bit[5] bit[4] Function 0 0 GPIO (default) 0 1 IO_SMI# (Note) 1 0 Reserved 1 1 Reserved See **Note 10.28** below.
6,7	GP13	Alternate Function Select bit[7] bit[6] Function 0 0 GPIO (default) 0 1 IRQIN1 (Note) 1 0 LED1 1 1 Reserved See **Note 10.29** below.

NOTE: If the Alternate Function is selected, the corresponding bits in the “GPIO Direction Registers” and ”GPIO Polarity Registers” must be configured accordingly.

Note 10.27 When the FDC_PP function is selected, the pin must be selected as an input. Polarity is controlled by the polarity bit. If enabled for PME or SMI, the interrupt is generated on either edge.

Note 10.28 Selecting the IO_SMI# function with GP12 configured with non-inverted polarity will give an active low output signal. The output type can be programmed for open drain via CR39.

Note 10.29 See Application Note in section 8.14.2 Routable IRQ Inputs.

10.4.65 CR45

CR45 can only be accessed in the configuration state and after the CSR has been initialized to 45H. The bits in this register are used to select an alternate function of GP16-GP17 pins.

Table 10.71 – CR45

GPIO ALTERNATE FUNCTION SELECT REGISTER 2		
TYPE: R/W		**DEFAULT:** 0x50 on VTR POR, BITS[7:4] VTR POR, VCC POR, and Hard Reset
BIT NO.	**BIT NAME**	**DESCRIPTION**
0,1	Reserved	Reads return 0.
2,3	Reserved	Reads return 0.
4,5	GP16	Alternate Function Select bit[5] bit[4] Function 0 0 GPIO 0 1 XA20 (default) - Note 1 0 Reserved 1 1 Reserved See **Note 10.30** below.
6,7	GP17	Alternate Function Select bit[7] bit[6] Function 0 0 GPIO 0 1 XA19 (default) – Note 1 0 Reserved 1 1 Reserved See **Note 10.31** below.

NOTE: If the Alternate Function is selected, the corresponding bits in the “GPIO Direction Registers” and ”GPIO Polarity Registers” must be configured accordingly.

Note 10.30 Bits[4:5] are reset on VTR POR, VCC POR, and Hard Reset.

Note 10.31 Bits[7:6] are reset on VTR, VCC, and Hard Reset.

10.4.66 CR46

CR46 can only be accessed in the configuration state and after the CSR has been initialized to 46H. The bits in this register are used to select an alternate function of GP20-GP23 pins.

Table 10.72 - CR46

GPIO ALTERNATE FUNCTION SELECT REGISTER 3		
TYPE: R/W		**DEFAULT:** 0x00 on VTR POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0,1	GP20	Alternate Function Select bit[1] bit[0] Function 0 0 GPIO (default) 0 1 IRRX2 1 0 IRQIN3 1 1 Reserved

GPIO ALTERNATE FUNCTION SELECT REGISTER 3		
TYPE: R/W		**DEFAULT:** 0x00 on VTR POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
2,3	GP21	Alternate Function Select bit[3] bit[2] Function 0 0 GPIO (default) 0 1 IRTX2 1 0 WDT 1 1 Reserved
4,5	GP22	Alternate Function Select bit[5] bit[4] Function 0 0 GPIO (default) 0 1 HPMODE (Note) 1 0 nXCS2 1 1 Reserved See **Note 10.32** below.
6,7	GP23	Alternate Function Select bit[7] bit[6] Function 0 0 GPIO (default) 0 1 LED2 1 0 IRQIN2 (Note) 1 1 Reserved

NOTE: If the Alternate Function is selected, the corresponding bits in the “GPIO Direction Registers” and ”GPIO Polarity Registers” must be configured accordingly.

Note 10.32 HPMODE is programmable in the IRQIN1/HPMODE/SIRQ_CLKRUN_En Configuration Register at offset CR29. The default HPMODE is the IRMODE function.

Note 10.33 See Application Note in section 8.14.2 Routable IRQ Inputs.

10.4.67 CR48

CR48 can only be accessed in the configuration state and after the CSR has been initialized to 48H. The bits in this register are used to select an alternate function of GP30-GP33 pins.

Table 10.73 - CR48

GPIO ALTERNATE FUNCTION SELECT REGISTER 5		
TYPE: R/W		**DEFAULT:** 0x00 on VTR POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0,1	GP30	Alternate Function Select bit[1] bit[0] Function 0 0 GPIO (default) 0 1 nRI3 1 0 Reserved 1 1 Reserved

GPIO ALTERNATE FUNCTION SELECT REGISTER 5		
TYPE: R/W		**DEFAULT:** 0x00 on VTR POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
2,3	GP31	Alternate Function Select bit[3] bit[2] Function 0 0 GPIO (default) 0 1 nDCD3 1 0 Reserved 1 1 Reserved
4,5	GP32	Alternate Function Select bit[5] bit[4] Function 0 0 GPIO (default) 0 1 nRXD3 1 0 Reserved 1 1 Reserved
6,7	GP33	Alternate Function Select bit[7] bit[6] Function 0 0 GPIO (default) 0 1 nTXD3 1 0 Reserved 1 1 Reserved

NOTE: If the Alternate Function is selected, the corresponding bits in the “GPIO Direction Registers” and ”GPIO Polarity Registers” must be configured accordingly.

10.4.68 CR49

CR49 can only be accessed in the configuration state and after the CSR has been initialized to 49H. The bits in this register are used to select an alternate function of GP34-GP37 pins.

Table 10.74 - CR49

GPIO ALTERNATE FUNCTION SELECT REGISTER 6		
TYPE: R/W		**DEFAULT:** 0x00 on VTR POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0,1	GP34	Alternate Function Select bit[1] bit[0] Function 0 0 GPIO (default) 0 1 nDSR3 1 0 Reserved 1 1 Reserved
2,3	GP35	Alternate Function Select bit[3] bit[2] Function 0 0 GPIO (default) 0 1 nRTS3 1 0 Reserved 1 1 Reserved

GPIO ALTERNATE FUNCTION SELECT REGISTER 6		
TYPE: R/W		**DEFAULT:** 0x00 on VTR POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
4,5	GP36	Alternate Function Select bit[5] bit[4] Function 0 0 GPIO (default) 0 1 nCTS3 1 0 Reserved 1 1 Reserved
6,7	GP37	Alternate Function Select bit[7] bit[6] Function 0 0 GPIO (default) 0 1 nDTR3 1 0 Reserved 1 1 Reserved

NOTE: If the Alternate Function is selected, the corresponding bits in the “GPIO Direction Registers” and ”GPIO Polarity Registers” must be configured accordingly.

10.4.69 CR4A

CR4A can only be accessed in the configuration state and after the CSR has been initialized to 4AH. The bits in this register are used to select an alternate function of GP40-GP43 pins.

Table 10.75 - CR4A

GPIO ALTERNATE FUNCTION SELECT REGISTER 7		
TYPE: R/W		**DEFAULT:** 0x00 on VTR POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0,1	GP40	Alternate Function Select bit[1] bit[0] Function 0 0 GPIO (default) 0 1 nRI4 1 0 Reserved 1 1 Reserved
2,3	GP41	Alternate Function Select bit[3] bit[2] Function 0 0 GPIO (default) 0 1 nDCD4 1 0 Reserved 1 1 Reserved
4,5	GP42	Alternate Function Select bit[5] bit[4] Function 0 0 GPIO (default) 0 1 nRXD4 1 0 Reserved 1 1 Reserved

GPIO ALTERNATE FUNCTION SELECT REGISTER 7		
TYPE: R/W		**DEFAULT:** 0x00 on VTR POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
6,7	GP43	Alternate Function Select bit[7] bit[6] Function 0 0 GPIO (default) 0 1 nTXD4 1 0 Reserved 1 1 Reserved

NOTE: If the Alternate Function is selected, the corresponding bits in the “GPIO Direction Registers” and ”GPIO Polarity Registers” must be configured accordingly.

10.4.70 CR4B

CR4B can only be accessed in the configuration state and after the CSR has been initialized to 4BH. The bits in this register are used to select an alternate function of GP44-GP47 pins.

Table 10.76 - CR4B

GPIO ALTERNATE FUNCTION SELECT REGISTER 8		
TYPE: R/W		**DEFAULT:** 0x00 on VTR POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0,1	GP44	Alternate Function Select bit[1] bit[0] Function 0 0 GPIO (default) 0 1 nDSR4 1 0 Reserved 1 1 Reserved
2,3	GP45	Alternate Function Select bit[3] bit[2] Function 0 0 GPIO (default) 0 1 nRTS4 1 0 Reserved 1 1 Reserved
4,5	GP46	Alternate Function Select bit[5] bit[4] Function 0 0 GPIO (default) 0 1 nCTS4 1 0 Reserved 1 1 Reserved
6,7	GP47	Alternate Function Select bit[7] bit[6] Function 0 0 GPIO (default) 0 1 nDTR4 1 0 Reserved 1 1 Reserved

NOTE: If the Alternate Function is selected, the corresponding bits in the “GPIO Direction Registers” and ”GPIO Polarity Registers” must be configured accordingly.

10.4.71 CR4C

CR4C can only be accessed in the configuration state and after the CSR has been initialized to 4CH. The bits in this register are used to select an alternate function of GP50-GP53 pins.

Table 10.77 - CR4C

GPIO ALTERNATE FUNCTION SELECT REGISTER 9		
TYPE: R/W		**DEFAULT:** 0x00 on VTR POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0,1	GP50	Alternate Function Select bit[1] bit[0] Function 0 0 GPIO (default) 0 1 nRI2 1 0 Reserved 1 1 Reserved
2,3	GP51	Alternate Function Select bit[3] bit[2] Function 0 0 GPIO (default) 0 1 nDCD2 1 0 Reserved 1 1 Reserved
4,5	GP52	Alternate Function Select bit[5] bit[4] Function 0 0 GPIO (default) 0 1 RXD2/IRRX 1 0 Reserved 1 1 Reserved
6,7	GP53	Alternate Function Select bit[7] bit[6] Function 0 0 GPIO (default) 0 1 TXD2/IRTX 1 0 Reserved 1 1 Reserved

NOTE: If the Alternate Function is selected, the corresponding bits in the “GPIO Direction Registers” and ”GPIO Polarity Registers” must be configured accordingly.

10.4.72 CR4D

CR4D can only be accessed in the configuration state and after the CSR has been initialized to 4DH. The bits in this register are used to select an alternate function of GP54-GP57 pins.

Table 10.78 – CR4D

GPIO ALTERNATE FUNCTION SELECT REGISTER 10		
TYPE: R/W		**DEFAULT:** 0x00 on VTR POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0,1	GP54	Alternate Function Select bit[1] bit[0] Function 0 0 GPIO (default) 0 1 nDSR2 1 0 Reserved 1 1 Reserved
2,3	GP55	Alternate Function Select bit[3] bit[2] Function 0 0 GPIO (default) 0 1 nRTS2 1 0 Reserved 1 1 Reserved
4,5	GP56	Alternate Function Select bit[5] bit[4] Function 0 0 GPIO (default) 0 1 nCTS2 1 0 Reserved 1 1 Reserved
6,7	GP57	Alternate Function Select bit[7] bit[6] Function 0 0 GPIO (default) 0 1 nDTR2 1 0 Reserved 1 1 Reserved

NOTE: If the Alternate Function is selected, the corresponding bits in the “GPIO Direction Registers” and ”GPIO Polarity Registers” must be configured accordingly.

10.4.73 CR4E

CR4E can only be accessed in the configuration state and after the CSR has been initialized to 4EH.

Table 10.79 - CR4E

X-BUS BASE I/O ADDRESS FOR CHIP SELECT 1 – HIGH BYTE		
TYPE: R/W when CR4F Bit[1] = 0 Read-Only when CR4F Bit[1] = 1		**DEFAULT:** 0x00 on VCC POR and Hard Reset
BIT NO.	**BIT NAME**	**DESCRIPTION**
0-3	Base Address High Byte	CR4E sets the high byte of the base I/O address for chip select 1. Bits [3:0] =address[11:8] Note: Bits[15:12] must be ‘0’ since the chip performs 16-bit address qualification on the base I/O addresses.
4-7	Reserved	Reads return 0.

10.4.74 CR4F

CR4F can only be accessed in the configuration state and after the CSR has been initialized to 4FH.

Table 10.80 - CR4F

X-BUS BASE ADDRESS FOR CHIP SELECT 1 – LOW BYTE		
TYPE: R/W when CR4F Bit[1] = 0 Read-Only when CR4F Bit[1] = 1		**DEFAULT:** 0x01 on VCC POR and Hard Reset
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	Disable bit	Bit[0] = Disable bit for nXCS1. 0=enable chip select 1=disable chip select (default)
1	Write Protect	Bit 1 is the write protect bit for registers CR4E and CR4F. Bit[1] = Register CR4E, CR4F Write Protect. Cleared by VCC POR and Hard Reset only. Cannot be cleared by software writing to this bit. 0=Register CR4E and CR4F are read/write 1=Register CR4E and CR4F are read-only
2-7	Base Address Low Byte	CR4F sets the Low byte of the base I/O address for chip select 1. Bits [7:2] are X-Bus mode dependent as follows: Mode 1: Bits [7:2] = address[7:2] Mode 2: Bits [7:4] = address[7:4] Bits [3:2] = These bits are R/W. They are not used in the address decode. Mode 3: Bits [7:3] = address[7:3] Bit [2] = address[1] Note: Bit [0] must be 0 for mode 3.

10.4.75 CR50

CR50 can only be accessed in the configuration state and after the CSR has been initialized to 50H.

Table 10.81 - CR50

X-BUS BASE ADDRESS FOR CHIP SELECT 2 – HIGH BYTE		
TYPE: R/W when CR50 Bit[1] = 0 Read-Only when CR51 Bit[1] = 1		**DEFAULT:** 0x00 on VCC POR and Hard Reset
BIT NO.	**BIT NAME**	**DESCRIPTION**
0-3	Base Address High Byte	CR50 sets the high byte of the base I/O address for chip select 2. Bits [3:0] = address[11:8] Note: Bits[15:12] must be '0' since the chip performs 16-bit address qualification on the base I/O addresses.
4-7	Reserved	Reads return 0.

10.4.76 CR51

CR51 can only be accessed in the configuration state and after the CSR has been initialized to 51H.

Table 10.82 - CR51

X-BUS BASE ADDRESS FOR CHIP SELECT 2 – LOW BYTE		
TYPE: R/W when CR51 Bit[1] = 0 Read-Only when CR51 Bit[1] = 1		**DEFAULT:** 0x01 on VCC POR and Hard Reset
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	Disable bit	Bit[0] = Disable bit for nXCS2. 0=enable chip select 1=disable chip select (default)
1	Write Protect	Bit [1] is the write protect bit for registers CR50 and CR51. Bit[1] = Register CR50, CR51 Write Protect. Cleared by VCC POR and Hard Reset only. Cannot be cleared by software writing to this bit. 0=Register CR50 and CR51 are read/write 1=Register CR50 and CR51 are read-only
2-7	Base Address Low Byte	CR51 sets the Low byte of the base I/O address for chip select 2. Bits [7:2] are X-Bus mode dependent as follows: Mode 1: Bits [7:2] = address[7:2] Mode 2: Bits [7:4] = address[7:4] Bits [3:2] = These bits are R/W. They are not used in the address decode. Mode 3: Bits [7:3] = address[7:3] Bit [2] = address[1] Note: Bit [0] must be 0 for mode 3.

10.4.77 CR52

CR52 can only be accessed in the configuration state and after the CSR has been initialized to 52H.

Table 10.83 - CR52

X-BUS I/O SELECT REGISTER		
TYPE: R/W when CR52 Bit[7] = 0 Read-Only when CR52 Bit[7] = 1		**DEFAULT:** 0x00 on VCC POR and Hard Reset
BIT NO.	**BIT NAME**	**DESCRIPTION**
0-1	X-Bus Mode	Bit [1:0] X-Bus Mode. 00=Mode 1 01=Mode 2 10=Mode 3 11=Reserved Note that the GPIOs must be configured properly to use the selected mode. The GPIOs are not automatically configured for the mode selected.

X-BUS I/O SELECT REGISTER		
TYPE: R/W when CR52 Bit[7] = 0 Read-Only when CR52 Bit[7] = 1		**DEFAULT:** 0x00 on VCC POR and Hard Reset
BIT NO.	**BIT NAME**	**DESCRIPTION**
2-3	Pulse Width Selection	Bits [3:2] X-Bus Read/Write Pulse Width Selection. These bits select the pulse width of the X-bus read and write strobes. They extend the LPC cycle accordingly by adding wait states (sync fields) into the cycle. 11=540nsec min 10=420nsec min 01=300nsec min 00=180nsec min (default)
4-6	Reserved	Reads return 0.
7	Register Write Protect	Bit [7] Register Write Protect. Cleared by VCC POR and Hard Reset only. Cannot be cleared by software writing this bit. 0=X-Bus selection register is Read/Write. 1=X-Bus Selection register is Read-Only

10.4.78 CR53

CR53 can only be accessed in the configuration state and after the CSR has been initialized to 53H.

Table 10.84 - CR53

X-BUS CHIP SELECT 0 REGISTER		
TYPE: R/W when CR53 Bit[0] = 0 Read-Only when CR53 Bit[0] = 1		**DEFAULT:** 0x8C on VCC POR and Hard Reset
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	Write Protect	Bits [0] = Write Protect for Chip Select 0 register (Note: Software cannot clear this bit.) 0=Register CR53 is read/write 1=Register CR53 is read-only
1	Reserved	Reads return 0.
2-3	Pulse Width Selection	Bits[3:2] X-Bus Read/Write Pulse Width Selection. These bits select the pulse width of the X-bus memory read and write strobes. They extend the LPC cycle accordingly by adding wait states (sync fields) into the cycle. 11=150nsec min (default) 10=120nsec min 01=90nsec min 00=60nsec min
4-6	Reserved	Reads return 0.
7	Enable	Bit [7] Enable for Chip Select 0 0=disable chip select 1=enable chip select

10.4.79 CR54

CR54 can only be accessed in the configuration state and after the CSR has been initialized to 54H.

Table 10.85 - CR54

FWH ID SELECT		
TYPE: R/W		**DEFAULT:** 0XX00000b on VCC POR and Hard Reset (Note: X = Strap Options)
BIT NO.	**BIT NAME**	**DESCRIPTION**
0-3	ID Select	Bits [3:0] ID Select Contains the FWH ID number. See Note 10.34 below.
4	IDSELEN	Bit[4] ID SELECT ENABLE 0=All FWH cycles will be claimed by FWH interface. 1=Only FWH cycles that contain ID values that match the value programmed in the ID Select bits will be claimed. All other FWH cycles will be ignored.
5	FWHSEL	Bit[5] FWH SELECT 0=LPC cycles are forwarded to X-Bus interface 1=FWH cycles are forwarded to X-Bus interface See Note 10.35 below.
6	MEMEN	Bit[6] MEMORY CYCLES ENABLED 0=Neither LPC memory or FWH cycles will be decoded for the X-Bus interface. 1=LPC memory cycles or FWH cycles will be decoded for the X-Bus interface depending on the status of the FWHSEL bit
7	Reserved	Read Only. A read returns 0

Note 10.34 If IDSELEN is asserted bits[3:0] are compared with the FWH ID and must match for the FWH cycle to be claimed.

Note 10.35 LPC and FWH cycles are only forwarded to X-Bus interface when the MEMEN bit is asserted ‘1’. FWHSEL can be set by a strap option.

Note 10.36 MEMEN can be set by a strap option.

10.5 Logical Device Base I/O Address and Range

Table 10.86 - I/O Base Address Configuration Register Description

LOGICAL DEVICE	REGISTER INDEX	BASE I/O RANGE (Note 10.37)	FIXED BASE OFFSETS
FDC	0x20	[0x0100:0x03F0] on 16-byte boundaries	+0 : SRA +1 : SRB +2 : DOR +3 : TDR +4 : MSR/DSR +5 : FIFO +7 : DIR/CCR
Parallel Port	0x23	[0x0100:0x03FC] on 4-byte boundaries (EPP Not supported) or [0x0100:0x03F8] on 8-byte boundaries	+0 : Data/ecpAfifo +1 : Status +2 : Control +400h : cfifo/ecpDfifo/tfifo/cnfgA +401h : cnfgB +402h : ecr
		(all modes supported, EPP is only available when the base address is on an 8-byte boundary)	+3 : EPP Address +4 : EPP Data 0 +5 : EPP Data 1 +6 : EPP Data 2 +7 : EPP Data 3
Serial Port 1	0x24	[0x0100:0x03F8] on 8 byte boundaries	+0 : RB/TB/LSB div +1 : IER/MSB div +2 : IIR/FCR +3 : LCR +4 : MCR +5 : LSR +6 : MSR +7 : SCR
Serial Port 2	0x25	[0x0100:0x03F8] on 8-byte boundaries	+0 : RB/TB/LSB div +1 : IER/MSB div +2 : IIR/FCR +3 : LCR +4 : MCR +5 : LSR +6 : MSR +7 : SCR
	0x2B (FIR/CIR)	[0x100:0x07F8] on 8-byte boundaries	+0 : DR/SCEA/CIRC/IDH/(IRDACR/BOFH) +1 : INTID/SCEB/CIRCR/IDL/BOFL +2 : IER/FIFOT/CIRBR/CID/BWCL +3 : LSR/LSA/VERN/(BWCH/TDSH) +4 : LCA/(IRQL/DMAC)/TDSL +5 : LCB/RDSH +6 : BS/RDSL +7 : MCR

LOGICAL DEVICE	REGISTER INDEX	BASE I/O RANGE (Note 10.37)	FIXED BASE OFFSETS
Runtime Register Block	0x30	[0x0100:0x0FE0] on 32-byte boundaries	+00 : PME_STS . . . +1B : PME_EN4 (See Table 9.1 in Chapter 9 Runtime Registers for Full List)
Config. Port	0x12, 0x13 (Note 2)	[0x0100:0x07FE] On 2-byte boundaries	See Configuration Registers in section 10.3 Configuration Registers Summary on page 162. They are accessed through the index and DATA ports located at the Configuration Port address and the Configuration Port address +1 respectively.
Serial Port 3	0x1B	[0x0100:0x03F8] on 8 byte boundaries	+0 : RB/TB/LSB div +1 : IER/MSB div +2 : IIR/FCR +3 : LCR +4 : MCR +5 : LSR +6 : MSR +7 : SCR
Serial Port 4	0x1C	[0x0100:0x03F8] on 8 byte boundaries	+0 : RB/TB/LSB div +1 : IER/MSB div +2 : IIR/FCR +3 : LCR +4 : MCR +5 : LSR +6 : MSR +7 : SCR
X-Bus	0x4E, 0x4F	Mode 1: [0x0000:0x0FFC] ON 4 BYTE BOUNDARIES Mode 2: [0x0000:0x0FF0] ON 16 BYTE BOUNDARIES Mode 3: [0x0000:0xFFE] ON 2 BYTE BOUNDARIES	+0: X-bus CS1 Address
	0x50, 0x51	Mode 1: [0x0000:0x0FFC] ON 4 BYTE BOUNDARIES Mode 2: [0x0000:0x0FF0] ON 16 BYTE BOUNDARIES Mode 3: [0x0000:0xFFE] ON 2 BYTE BOUNDARIES	+0: X-bus CS2 Address

Note 10.37 The Configuration Port is at either 0x02E or 0x04E (for SYSOPT=0 or SYSOPT=1) at power up and can be relocated via CR12 and CR13.

10.6 Note A. Logical Device IRQ and DMA Operation

1) IRQ and DMA Enable and Disable: Any time the IRQ or DMA channel for a logical block is disabled by a register bit in that logical block, the IRQ and/or DMA channel is disabled. This is in addition to the IRQ and DMA channel disabled by the Configuration Registers (active bit or address not valid).

   a) FDC:

   For the following cases, the IRQ and DMA channel used by the FDC are disabled. Digital Output Register (Base+2) bit D3 (DMAEN) set to "0". The FDC is in power down (disabled).

   b) Serial Ports:

   Modem Control Register (MCR) Bit D2 (OUT2) - When OUT2 is a logic "0", the serial port interrupts disabled. Disabling DMA Enable bit, disables DMA for UART2. Refer to the IrCC specification.

   c) Parallel Port:

   i. SPP and EPP modes: Control Port (Base+2) bit D4 (IRQE) set to "0", IRQ is disabled.

   ii. ECP Mode:

   1) (DMA) dmaEn from ecr register. See Table 10.87 below.

   2) IRQ - See Table 10.87 below.

Table 10.87 - IRQ & DMA Operation in ECP Mode

MODE (FROM ECR REGISTER)		IRQ CONTROLLED BY	DMA CONTROLLED BY
000	PRINTER	IRQE	dmaEn
001	SPP	IRQE	dmaEn
010	FIFO	(on)	dmaEn
011	ECP	(on)	dmaEn
100	EPP	IRQE	dmaEn
101	RES	IRQE	dmaEn
110	TEST	(on)	dmaEn
111	CONFIG	IRQE	dmaEn

Chapter 11 Operational Description

11.1 Maximum Guaranteed Ratings

Operating Temperature Range ..... 0^oC to $+70^oC$
Storage Temperature Range ..... -55^o to $+150^oC$
Lead Temperature Range ..... Refer to JEDEC Spec. J-STD-020
Positive Voltage on any pin, with respect to Ground ..... V_{CC}+0.3V
Negative Voltage on any pin, with respect to Ground ..... -0.3V
Maximum V_{CC} ..... +5.5V

NOTE: Stresses above those listed above could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

11.2 DC Electrical Characteristics

(T_A = 0^0C – 70^0C, V_{CC} = +3.3 V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
I Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
IS Type Input Buffer						
Low Input Level	V_{ILIS}			0.8	V	Schmitt Trigger
High Input Level	V_{IHIS}	2.2			V	Schmitt Trigger
Schmitt Trigger Hysteresis	V_{HYS}		100		mV	
IPD Type Input Buffer						
Low Input Level	V_{ILIPD}			0.8	V	TTL Levels
High Input Level	V_{IHIPD}	2.0			V	
Internal Pulldown			30		µA	

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
Input Leakage, I and IS Buffers						
Low Input Leakage	I_{IL}	-10		+10	µA	V_{IN} = 0
High Input Leakage	I_{IH}	-10		+10	µA	V_{IN} = V_{CC}
O6 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 6mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -3mA
IO8 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -4mA
Leakage Current	I_{LEAK}			±10	µA	V_{IN} = 0 to V_{CC} (**Note 11.1**)
O8 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -4mA
OD8 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8mA
Leakage Current	I_{LEAK}			+10	µA	V_{IN} = 0 to V_{CC}
O12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -6mA
IO12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -6mA
Leakage Current	I_{LEAK}			±10	µA	V_{IN} = 0 to V_{CC} (**Note 11.1**)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
OD12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA
Leakage Current	I_{LEAK}			+10	µA	V_{IN} = 0 to V_{CC}
OD14 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 14mA
Leakage Current	I_{LEAK}			+10	µA	V_{IN} = 0 to V_{CC}
OP14 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 14mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -14mA
Leakage Current	I_{LEAK}			+10	µA	V_{IN} = 0 to V_{CC} (**Note 11.1**)
IOP14 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 14mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -14mA
Leakage Current	I_{LEAK}			±10	µA	V_{IN} = 0 to V_{CC} (**Note 11.1**)
Backdrive Protect/ChiProtect (All pins excluding LAD[3:0], LDRQ#, LPCPD#, LFRAME#)	I_{IL}			± 10	µA	V_{CC} = 0V V_{IN} = 5.5V Max
5V Tolerant Pins (All pins excluding LAD[3:0], LDRQ#, LPCPD#, LFRAME#) Inputs and Outputs in High Impedance State	I_{IL}			± 10	µA	V_{CC} = 3.3V V_{IN} = 5.5V Max
LPC Bus Pins (LAD[3:0], LDRQ#, LPCPD#, LFRAME#)	I_{IL}			± 10	µA	V_{CC} = 0V and V_{CC} = 3.3V V_{IN} = 3.6V Max
V_{CC} Supply Current Active	I_{CC}			17 (**Note 11.2**)	mA	All outputs open, all inputs transitioning from/to 0V to/from 3.3V
Trickle Supply Voltage	V_{TR}	V_{CC} min -.5V (**Note 11.4**)		V_{CC} max	V	V_{CC} must not be greater than .5V above V_{TR}

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
V_{TR} Supply Current Active	I_{TR}			0.2 (**Note 11.2**, **Note 11.3**)	mA	All outputs open, all inputs transitioning from/to 0V to/from 3.3V

Note 11.1 All output leakage's are measured with all pins in high impedance.

Note 11.2 These values are estimated. They will be updated after characterization. Contact SMSC for the latest values.

Note 11.3 Max I_{TR} with V_{CC} = 3.3V (nominal) is 0.2mA. Max I_{TR} with V_{CC} = 0V (nominal) is 60µA.

Note 11.4 The minimum value given for V_{TR} applies when V_{CC} is active. When V_{CC} is 0V, the minimum V_{TR} is 0V.

CAPACITANCE T_A = 25^{0}C; fc = 1MHz; V_{CC} = 3.3V ±10%

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITION
		MIN	TYP	MAX		
Clock Input Capacitance	C_{IN}			20	pF	All pins except pin under test tied to AC ground
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

Chapter 12 Timing Diagrams

For the Timing Diagrams shown, the following capacitive loads are used on outputs.

NAME	CAPACITANCE TOTAL (pF)
SER_IRQ	50
nLAD[3:0]	50
LDRQ#	50
nDIR	240
nSTEP	240
nDS0-1	240
nWDATA	240
PD[0:7]	240
nSTROBE	240
nALF	240
SLCTIN	240
TXD1	50
TXD2	50
CLKRUN#	50
nXCS[0:2]	50
XA[0:20]	50
XD[0:7]	50
nXRD	50
nXWR	50

12.1 Power-up Timing

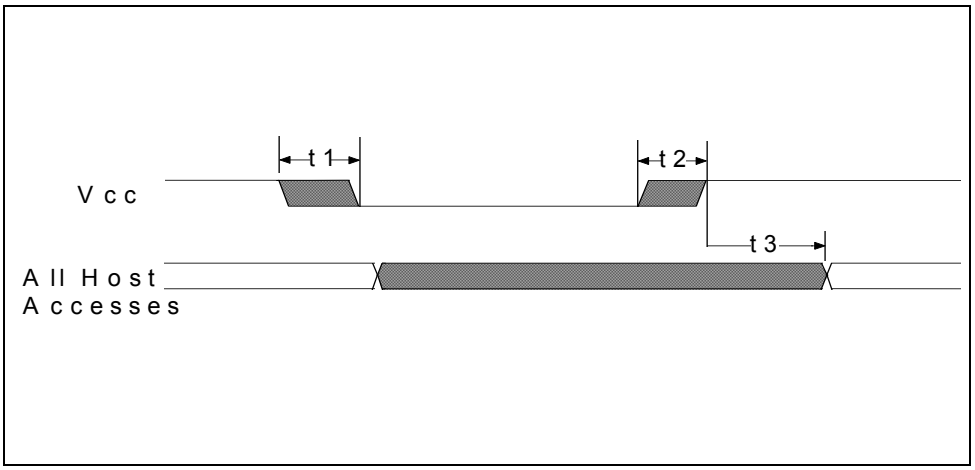


Figure 12.1 - Power-Up Timing

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Vcc Slew from 2.7V to 0V	300			µs
t2	Vcc Slew from 0V to 2.7V	100			µs
t3	All Host Accesses After Powerup (**Note 12.1**)	125		500	µs

Note 12.1 Internal write-protection period after Vcc passes 2.7 volts on power-up.

12.2 Input Clock Timing

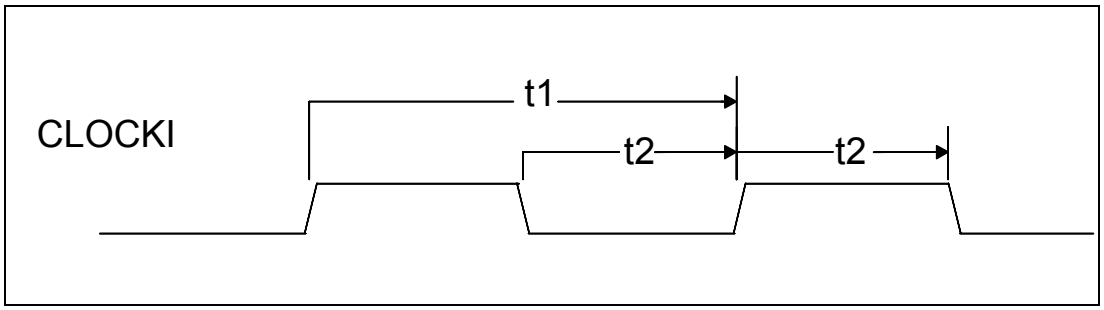


Figure 12.2 – 14MHZ Clock Timing

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Clock Cycle Time for 14.318MHZ		69.84		ns
t2	Clock High Time/Low Time for 14.318MHz	20	35		ns
	Clock Rise Time/Fall Time (not shown)			5	ns

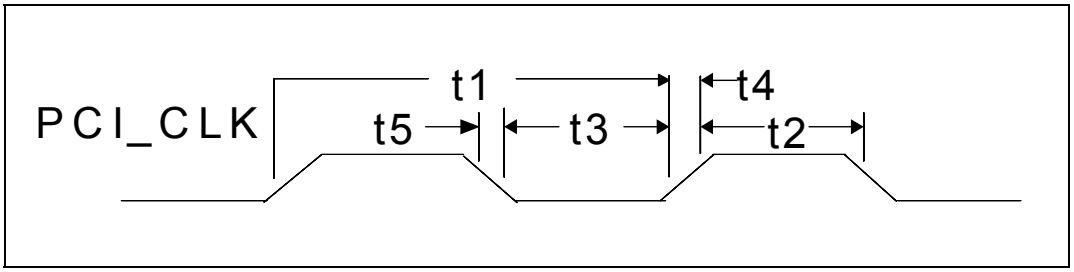


Figure 12.3 – PCI Clock Timing

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Period	30		33.3	nsec
t2	High Time	12			nsec
t3	Low Time	12			nsec
t4	Rise Time			3	nsec
t5	Fall Time			3	nsec

12.3 LPC Timing (LPC Mode Only)

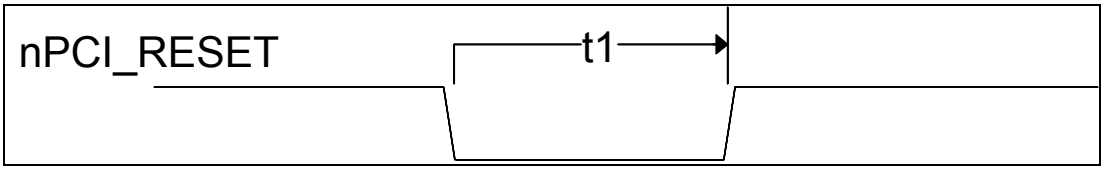


Figure 12.4 - Reset Timing

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	PCI_RESET# width	1			ms

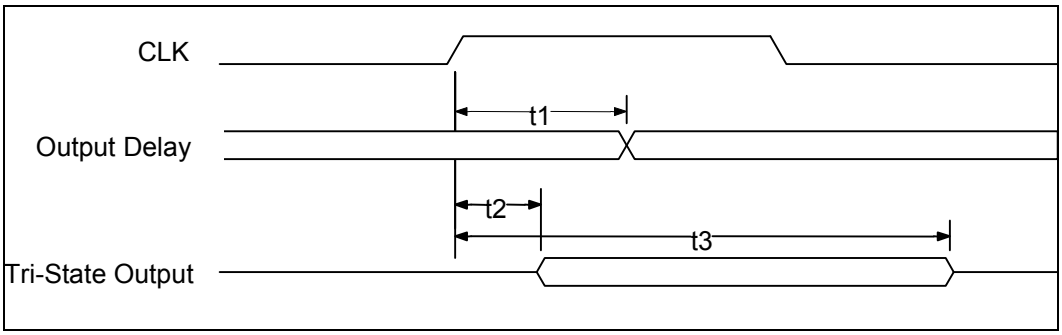


Figure 12.5 - Output Timing Measurement Conditions, LPC Signals

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	CLK to Signal Valid Delay – Bused Signals	2		11	ns
t2	Float to Active Delay	2		11	ns
t3	Active to Float Delay			28	ns

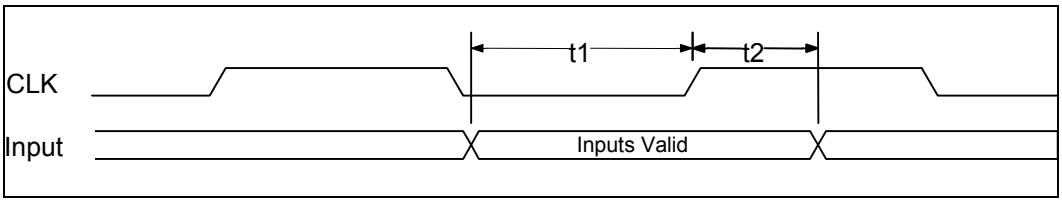
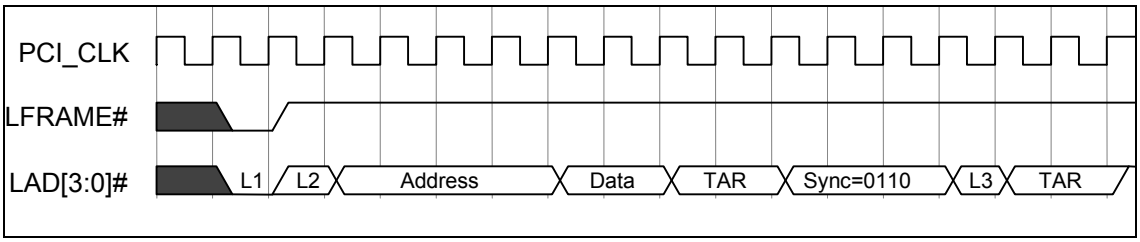


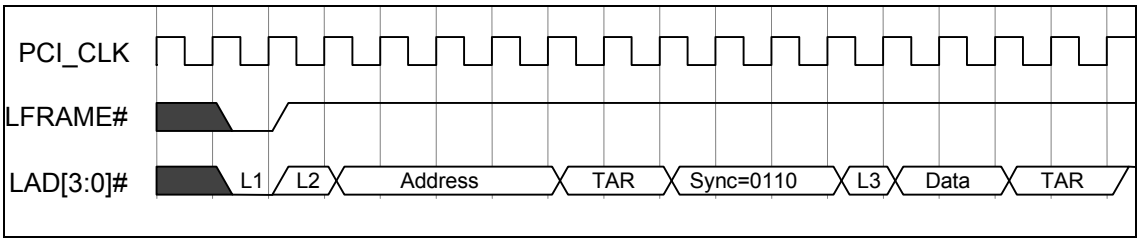
Figure 12.6 – Input Timing Measurement Conditions, LPC Signals

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Input Set Up Time to CLK – Bused Signals	7			ns
t2	Input Hold Time from CLK	0			ns



NOTE: L1=Start; L2=CYCTYP+DIR; L3=Sync of 0000

Figure 12.7 - I/O Write



NOTE: L1=Start; L2=CYCTYP+DIR; L3=Sync of 0000

Figure 12.8 - I/O Read

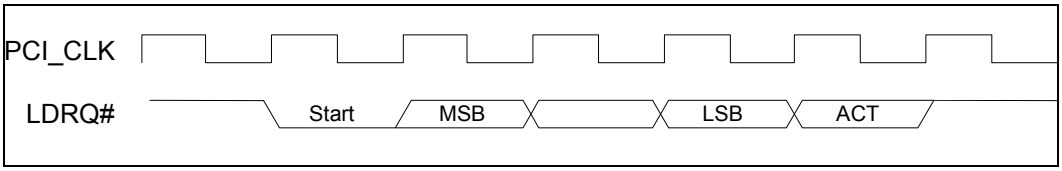
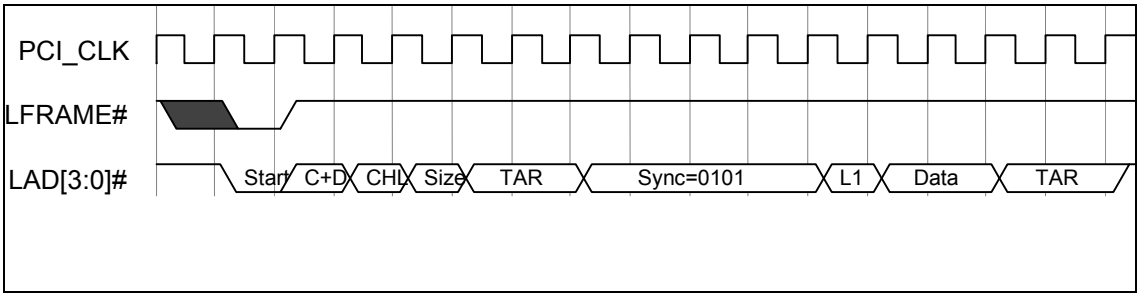
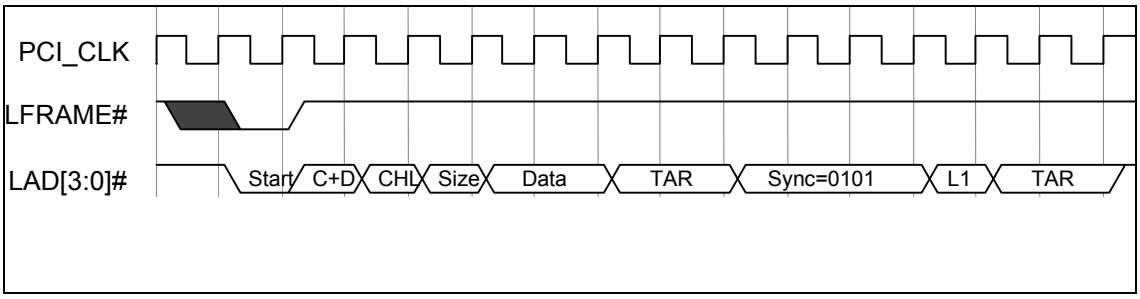


Figure 12.9 - DMA Request Assertion Through LDRQ#



NOTE: L1=Sync of 0000

Figure 12.10 – DMA Write (First Byte)



NOTE: L1=Sync of 0000

Figure 12.11 - DMA Read (First Byte)

12.4 X-Bus Timing (LPC Mode Only)

12.4.1 X-Bus I/O Timing

NOTE: The following timing values are based on a 33MHz PCI clock. Timing values will vary with variations in the PCI clock frequency.

12.4.1.1 X-Bus I/O Read Timing

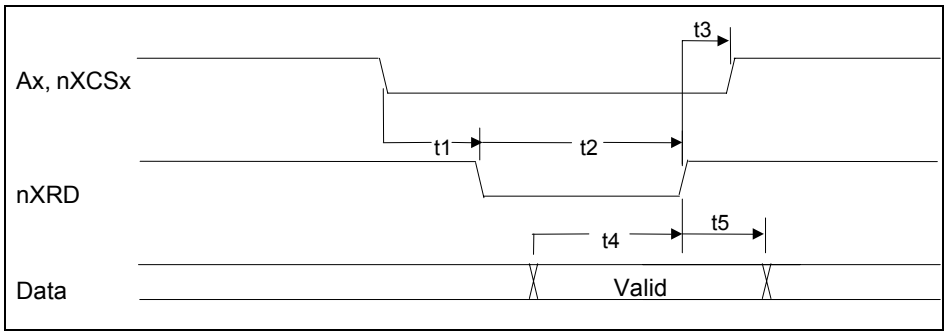


Figure 12.12 – X-Bus I/O Read Timing

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	nXCS active to nXRD active	100		190	ns
t2	nXRD active to nXRD inactive	A: 180 B: 300 C: 420 D: 540			ns
t3	nXRD inactive to nxCS inactive	40			ns
t4	Data valid to nXRD inactive	20			ns
t5	nXRD inactive to data invalid	0			ns

NOTE: Cases A-D for t2 correspond to the different pulse width options for the X-Bus read strobe. See the Pulse Width Selection bits located in the X-Bus I/O Select Register at offset CR52.

12.4.1.2 X-Bus I/O Write Timing

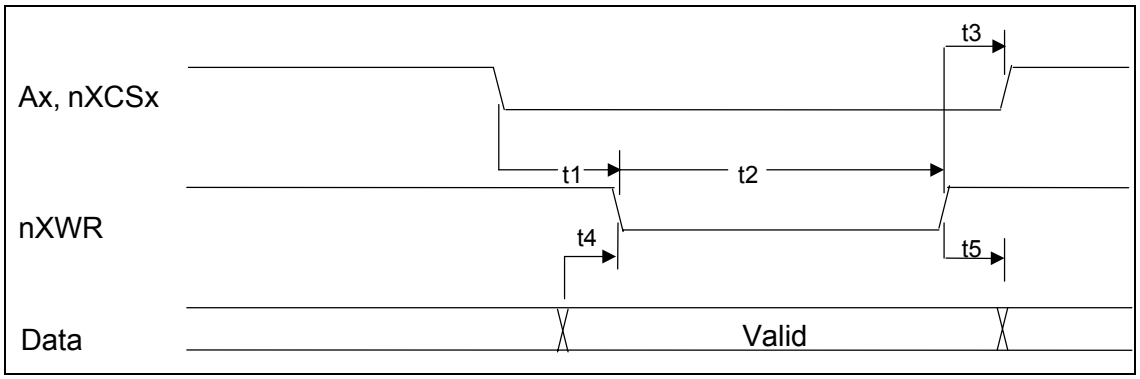


Figure 12.13 - X-Bus Write Timing

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	nXCS active to nXWR active	100		190	ns
t2	nXWR active to nXWR inactive	A: 180 B: 300 C: 420 D: 540			ns
t3	nXWR inactive to nXCS inactive	40			ns
t4	Data valid to nXWR active	22			ns
t5	nXWR inactive to data invalid	45			ns

NOTE: Cases A-D for t2 correspond to the different pulse width options for the X-Bus write strobe. See the Pulse Width Selection bits located in the X-Bus I/O Select Register at offset CR52.

12.4.2 Representative LPC I/O Cycle to X-Bus Cycle Timing

12.4.2.1 X-Bus I/O Read Cycle: LPC I/O Read Cycle – Data from X-Bus Device to Host

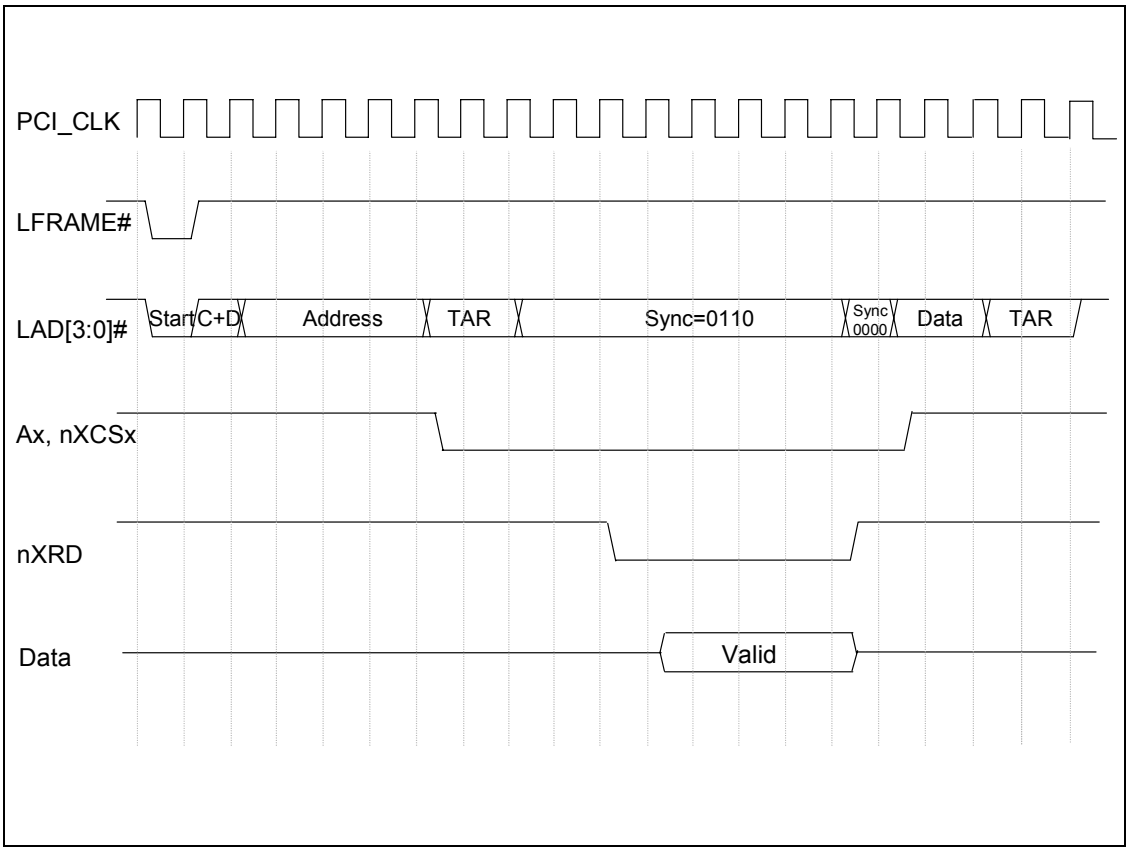


Figure 12.14 – X-Bus and LPC I/O Read Cyle

NOTE: Minimum read pulse width is shown.

12.4.2.2 X-Bus I/O Write Cycle: LPC I/O Write Cycle - Data from Host to X-Bus Device

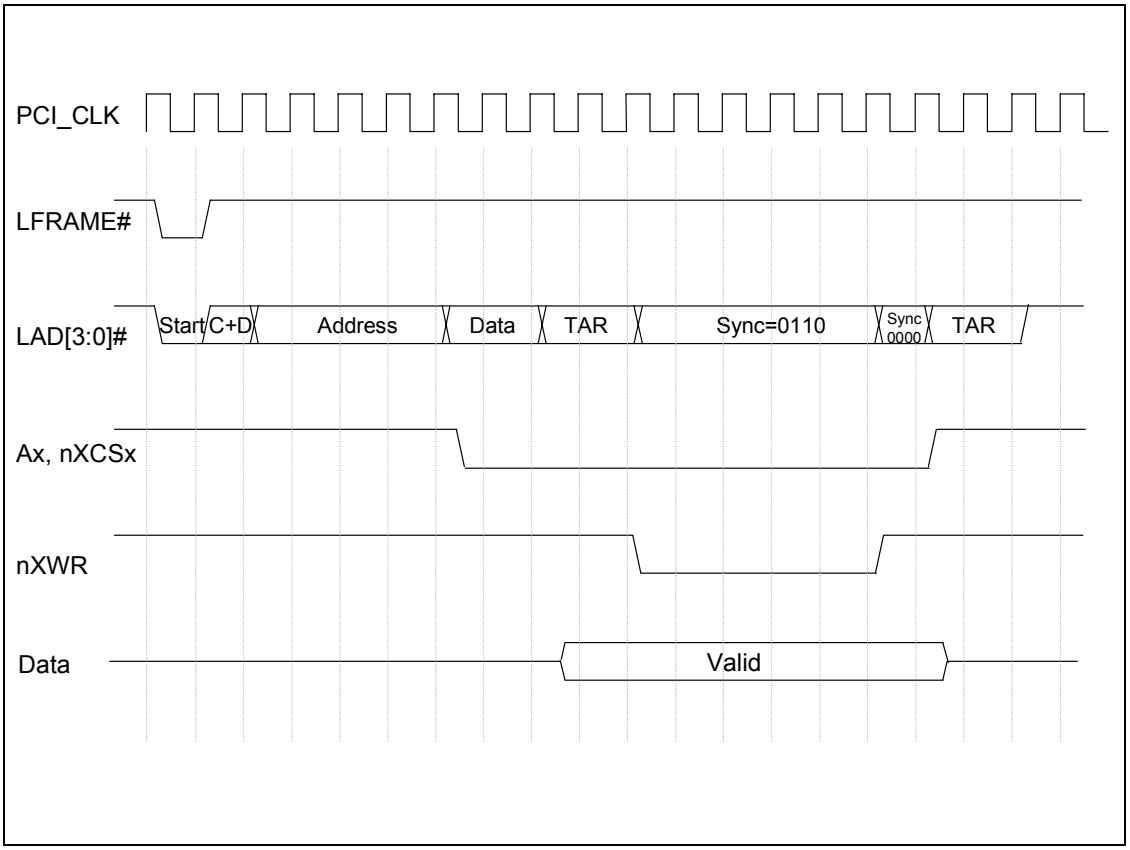


Figure 12.15 – X-Bus and LPC I/O Write Cycle

NOTE: Minimum write pulse width is shown.

12.4.3 X-Bus Memory Cycle Timing

The following timing values are based on a 33MHz PCI clock. Timing values will vary with variations in the PCI clock frequency.

The following timing diagrams are designed to support Intel's 3 Volt Strata Flash Memory devices.

12.4.3.1 Timing For FWH and LPC initiated Memory Read Cycles with the X-Bus

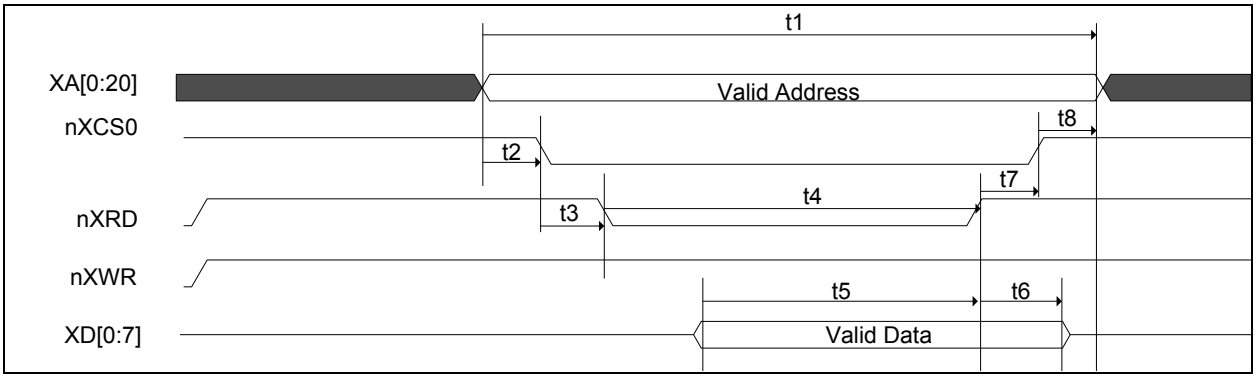


Figure 12.16 - X-Bus Memory Read

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Valid Address	70		-	ns
t2	Valid Address to Chip Select active	0		30	ns
t3	Chip Select active to nXRD active	10		40	ns
t4	nXRD active to nXRD inactive	A: 60 B: 90 C: 120 D: 150		A: 70 B: 100 C: 130 D: 160	ns
t5	Data Valid to nXRD inactive	20		-	ns
t6	Data Hold following nXRD inactive	0		30	ns
t7	nXRD inactive to Chip Select inactive	0		10	ns
t8	Address Hold following Chip Select inactive	0		-	ns

12.4.3.2 Timing For FWH and LPC initiated Memory Write Cycles with the X-Bus

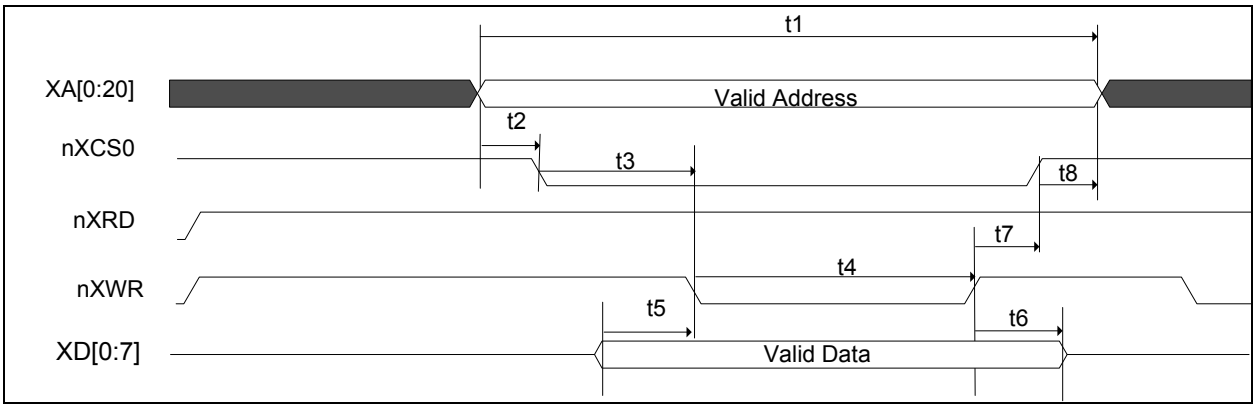
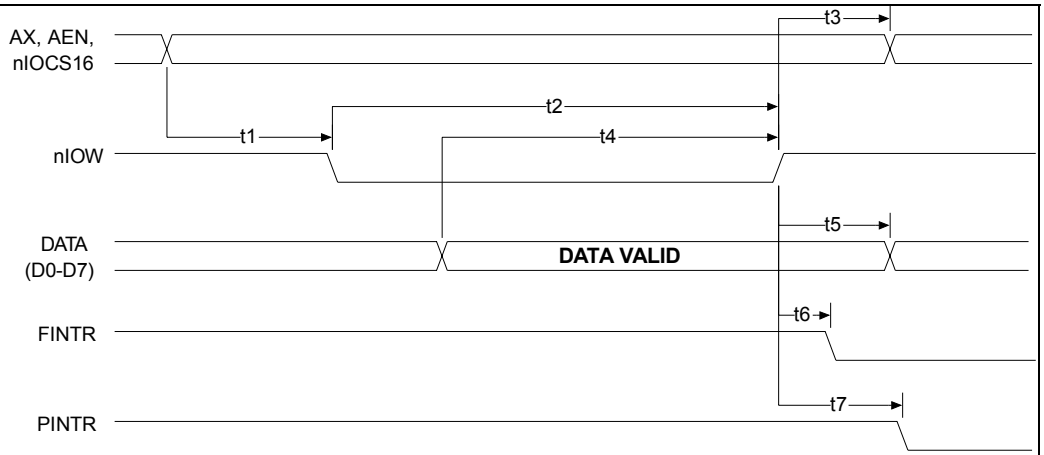


Figure 12.17 – X-Bus Memory Write

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Valid Address	80		-	ns
t2	Valid Address to Chip Select active	0		30	ns
t3	Chip Select active to nXWR active	10		40	ns
t4	nXWR active to nXWR inactive	A: 60 B: 90 C: 120 D: 150		A: 70 B: 100 C: 130 D: 160	ns
t5	Data Valid to nXWR active	10		40	ns
t6	Data Hold following nXWR inactive	10		40	ns
t7	nXWR inactive to nXCS[x] inactive	10		40	ns
t8	Address Hold following nXCS[x] inactive	0		-	ns

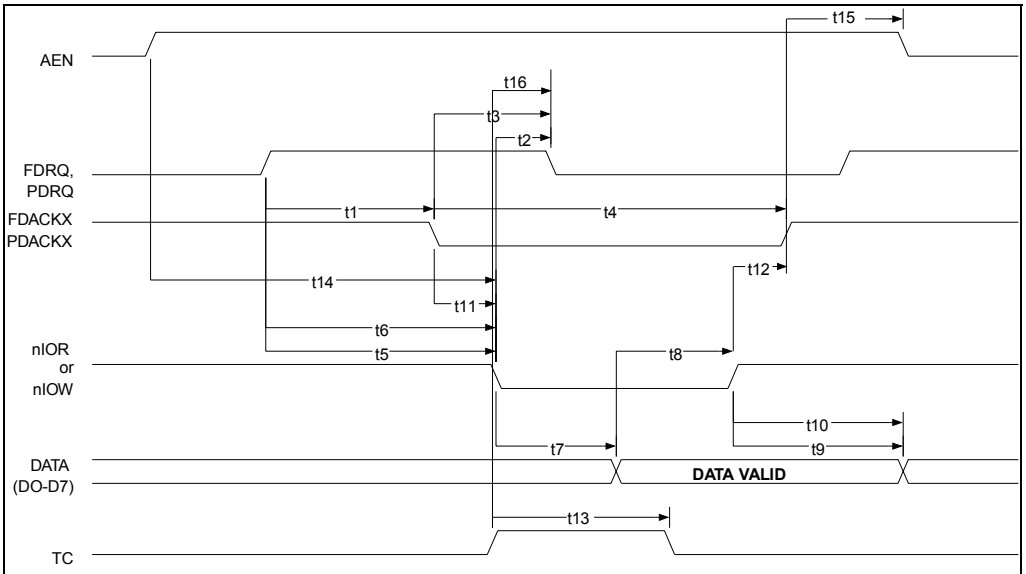
12.5 Host Timing (ISA Mode Only)



PINTR is the interrupt assigned to the Parallel Port
FINTR is the interrupt assigned to the Floppy Disk

	Parameter	min	typ	max	units
t1	A0-A9, AEN, nIOCS16 Set Up to nIOW Low	40			ns
t2	nIOW Width	150			ns
t3	A0-A9, AEN, nIOCS16 Hold from nIOW High	10			ns
t4	Data Set Up Time to nIOW High	40			ns
t5	Data Hold Time from nIOW High	10			ns
t6	Write Strobe to Clear FINTR		40	55	ns
t7	nIOW Inactive to PINTR Inactive			260	ns

Figure 12.18 - Microprocessor Write Timing



FDRQ refers to the DRQ assigned to the Floppy Disk
PDRQ refers to the DRQ assigned to the Parallel Port
FDACKX refers to the nDACK assigned to the to the Floppy Disk
PDACKX refers to the nDACK assigned to the Parallel Port

	Parameter	min	typ	max	units
t1	nDACK Delay Time from FDRQ High	0			ns
t2	DRQ Reset Delay from nIOR or nIOW			100	ns
t3	FDRQ Reset Delay from nDACK Low			100	ns
t4	nDACK Width	150			ns
t5	nIOR Delay from FDRQ High	0			ns
t6	nIOW Delay from FDRQ High	0			ns
t7	Data Access Time from nIOR Low			100	ns
t8	Data Set Up Time to nIOW High	40			ns
t9	Data to Float Delay from nIOR High			60	ns
t10	Data Hold Time from nIOW High	10			ns
t11	nDACK Set Up to nIOW/nIOR Low	10			ns
t12	nDACK Hold After nIOW/nIOR High	5			ns
t13	TC Pulse Width	10			ns
t14	AEN Set Up to nIOR/nIOW	60			ns
t15	AEN Hold from nDACK	40			ns
t16	TC Active to PDRQ Inactive	10		100	ns

Figure 12.19 - DMA Timing

12.6 Floppy Disk Timing

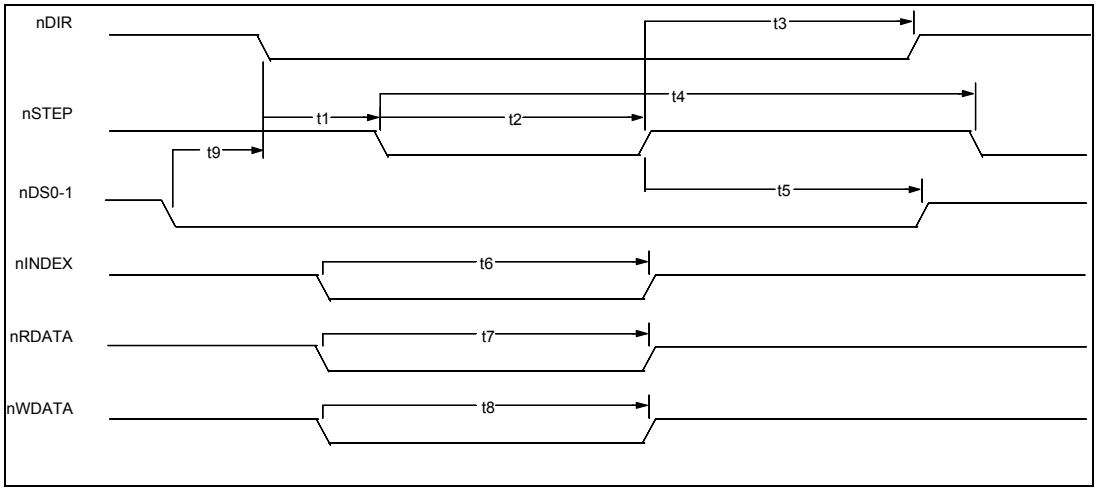


Figure 12.20 – Floppy Disk Drive Timing (AT Mode Only)

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	nDIR Set Up to STEP Low		4		X (**Note 12.2**)
t2	nSTEP Active Time Low		24		X (**Note 12.2**)
t3	nDIR Hold Time after nSTEP		96		X (**Note 12.2**)
t4	nSTEP Cycle Time		132		X (**Note 12.2**)
t5	nDS0-1 Hold Time from nSTEP Low (**Note 12.3**)		20		X (**Note 12.2**)
t6	nINDEX Pulse Width		2		X (**Note 12.2**)
t7	nRDATA Active Time Low		40		ns
t8	nWDATA Write Data Width Low		.5		Y (**Note 12.2**)
t9	nDS0-1, Setup Time nDIR Low (**Note 12.3**)	0			ns

Note 12.2 X specifies one MCLK period and Y specifies one WCLK period. MCLK = 16 x Data Rate (at 500 kb/s MCLK = 8 MHz) WCLK = 2 x Data Rate (at 500 kb/s WCLK = 1 MHz)

Note 12.3 The nDS0-1 setup and hold times must be met by software.

12.7 EPP Parallel Port Timing

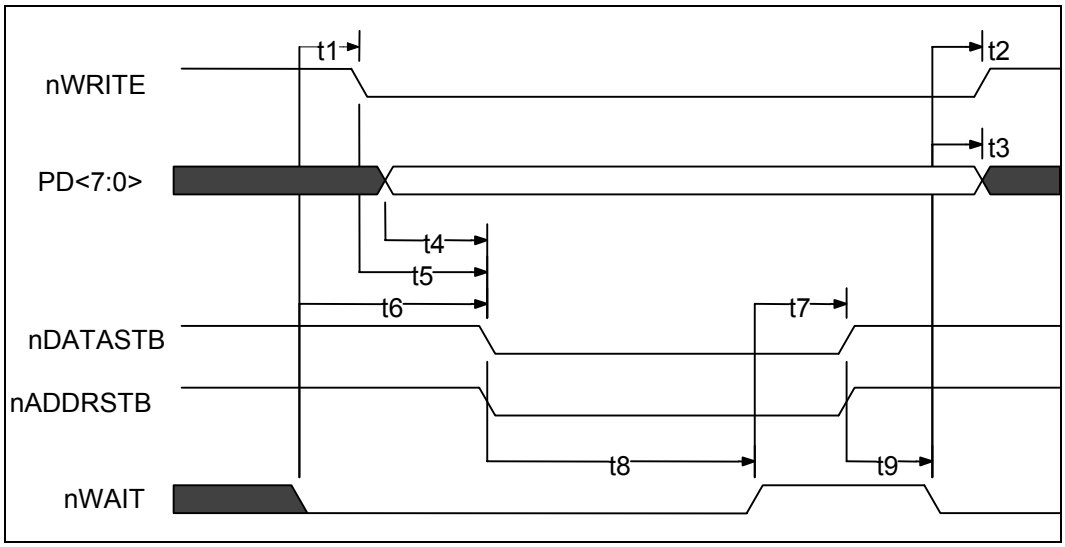


Figure 12.21 - EPP 1.9 Data or Address Write Cycle

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	nWAIT Asserted to nWRITE Asserted (Note 12.4)	60		185	ns
t2	nWAIT Asserted to nWRITE Change (Note 12.4)	60		185	ns
t3	nWAIT Asserted to PDATA Invalid (Note 12.4)	0			ns
t4	PDATA Valid to Command Asserted	10			ns
t5	nWRITE to Command Asserted	5		35	ns
t6	nWAIT Asserted to Command Asserted (Note 12.4)	60		210	ns
t7	nWAIT Deasserted to Command Deasserted (Note 12.4)	60		190	ns
t8	Command Asserted to nWAIT Deasserted	0		10	µs
t9	Command Deasserted to nWAIT Asserted	0			ns

Note 12.4 nWAIT must be filtered to compensate for ringing on the parallel bus cable. WAIT is considered to have settled after it does not transition for a minimum of 50 nsec.

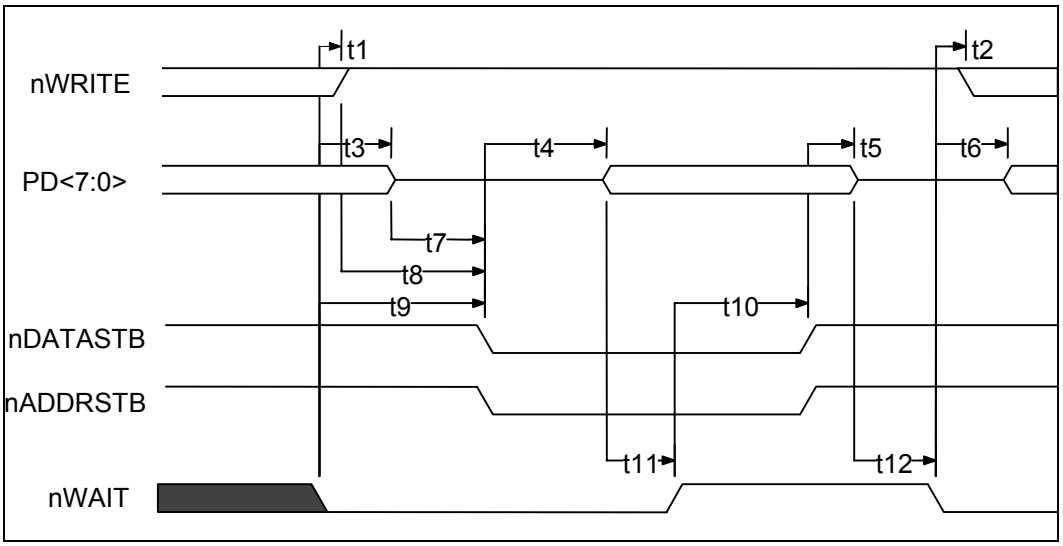


Figure 12.22 - EPP 1.9 Data or Address Read Cycle

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	nWAIT Asserted to nWRITE Deasserted	0		185	ns
t2	nWAIT Asserted to nWRITE Modified (**Note 12.5**, **Note 12.6**)	60		190	ns
t3	nWAIT Asserted to PDATA Hi-Z (**Note 12.5**)	60		180	ns
t4	Command Asserted to PDATA Valid	0			ns
t5	Command Deasserted to PDATA Hi-Z	0			ns
t6	nWAIT Asserted to PDATA Driven (**Note 12.5**)	60		190	ns
t7	PDATA Hi-Z to Command Asserted	0		30	ns
t8	nWRITE Deasserted to Command	1			ns
t9	nWAIT Asserted to Command Asserted	0		195	ns
t10	nWAIT Deasserted to Command Deasserted (**Note 12.5**)	60		180	ns
t11	PDATA Valid to nWAIT Deasserted	0			ns
t12	PDATA Hi-Z to nWAIT Asserted	0			µs

Note 12.5 nWAIT is considered to have settled after it does not transition for a minimum of 50 ns.

Note 12.6 When not executing a write cycle, EPP nWRITE is inactive high.

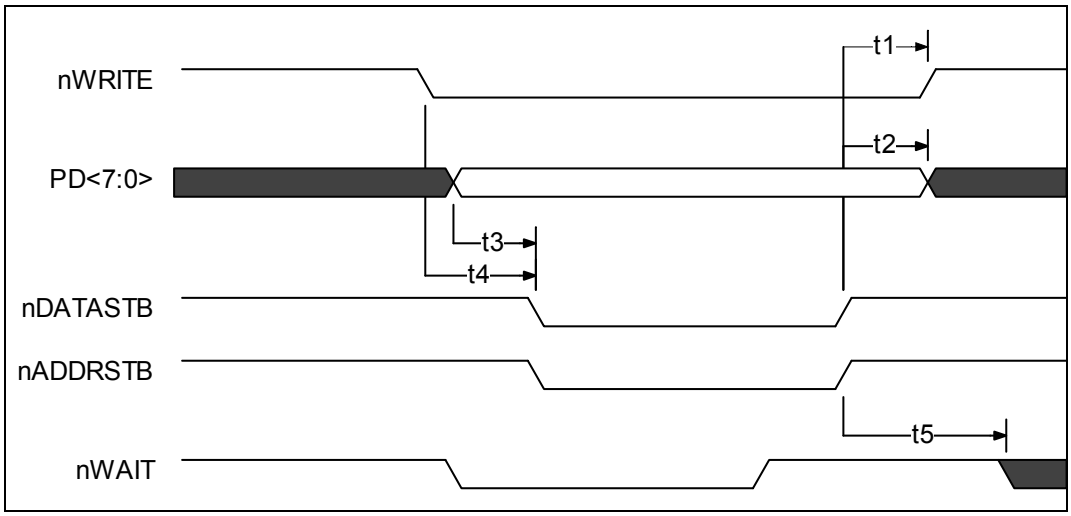


Figure 12.23 - EPP 1.7 Data or Address Write Cycle

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Command Deasserted to nWRITE Change	0		40	ns
t2	Command Deasserted to PDATA Invalid	50			ns
t3	PDATA Valid to Command Asserted	10		35	ns
t4	nWRITE to Command	5		35	ns
t5	Command Deasserted to nWAIT Deasserted	0			ns

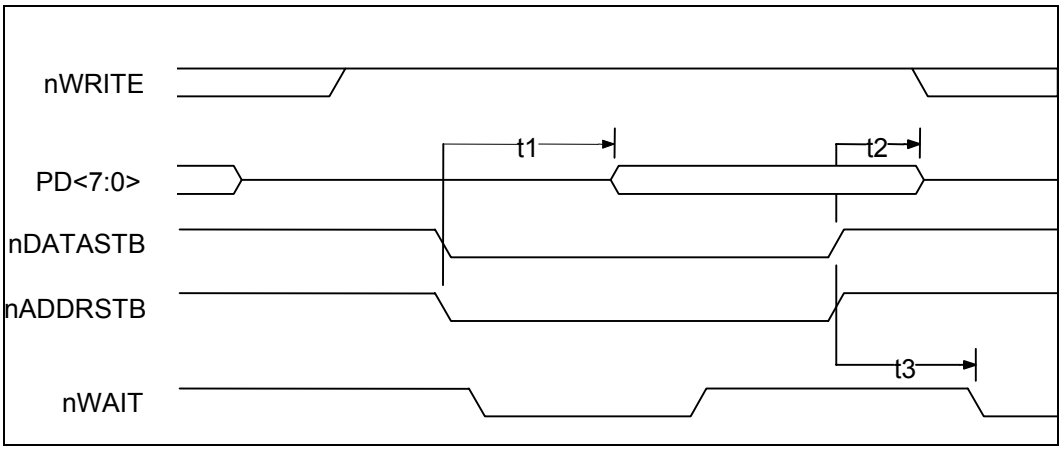


Figure 12.24 - EPP 1.7 Data or Address Read Cycle

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Command Asserted to PDATA Valid	0			ns
t2	Command Deasserted to PDATA Hi-Z	0			ns
t3	Command Deasserted to nWAIT Deasserted	0			ns

12.8 ECP Parallel Port Timing

12.8.1 Parallel Port FIFO (Mode 101)

The standard parallel port is run at or near the peak 500KBytes/sec allowed in the forward direction using DMA. The state machine does not examine nACK and begins the next transfer based on Busy. Refer to Figure 12.25.

12.8.2 ECP Parallel Port Timing

The timing is designed to allow operation at approximately 2.0 Mbytes/sec over a 15ft cable. If a shorter cable is used then the bandwidth will increase.

12.8.3 Forward-Idle

When the host has no data to send it keeps HostClk (nStrobe) high and the peripheral will leave PeriphClk (Busy) low.

12.8.4 Forward Data Transfer Phase

The interface transfers data and commands from the host to the peripheral using an interlocked PeriphAck and HostClk. The peripheral may indicate its desire to send data to the host by asserting nPeriphRequest.

The Forward Data Transfer Phase may be entered from the Forward-Idle Phase. While in the Forward Phase the peripheral may asynchronously assert the nPeriphRequest (nFault) to request that the channel be reversed. When the peripheral is not busy it sets PeriphAck (Busy) low. The host then sets HostClk (nStrobe) low when it is prepared to send data. The data must be stable for the specified setup time prior to the falling edge of HostClk. The peripheral then sets PeriphAck (Busy) high to acknowledge the handshake. The host then sets HostClk (nStrobe) high. The peripheral then accepts the data and sets PeriphAck (Busy) low, completing the transfer. This sequence is shown in Figure 12.26.

The timing is designed to provide 3 cable round-trip times for data setup if Data is driven simultaneously with HostClk (nStrobe).

12.8.5 Reverse-Idle Phase

The peripheral has no data to send and keeps PeriphClk high. The host is idle and keeps HostAck low.

12.8.6 Reverse Data Transfer Phase

The interface transfers data and commands from the peripheral to the host using an interlocked HostAck and PeriphClk.

The Reverse Data Transfer Phase may be entered from the Reverse-Idle Phase. After the previous byte has beed accepted the host sets HostAck (nALF) low. The peripheral then sets PeriphClk (nACK) low when it has data to send. The data must be stable for the specified setup time prior to the falling edge of PeriphClk. When the host is ready to accept a byte it sets HostAck (nALF) high to acknowledge the

handshake. The peripheral then sets PeriphClk (nACK) high. After the host has accepted the data it sets HostAck (nALF) low, completing the transfer. This sequence is shown in Figure 12.27.

12.8.7 Output Drivers

To facilitate higher performance data transfer, the use of balanced CMOS active drivers for critical signals (Data, HostAck, HostClk, PeriphAck, PeriphClk) are used in ECP Mode. Because the use of active drivers can present compatibility problems in Compatible Mode (the control signals, by tradition, are specified as open-drain), the drivers are dynamically changed from open-drain to push-pull. The timing for the dynamic driver change is specified in then IEEE 1284 Extended Capabilities Port Protocol and ISA Interface Standard, Rev. 1.14, July 14, 1993, available from Microsoft. The dynamic driver change must be implemented properly to prevent glitching the outputs.

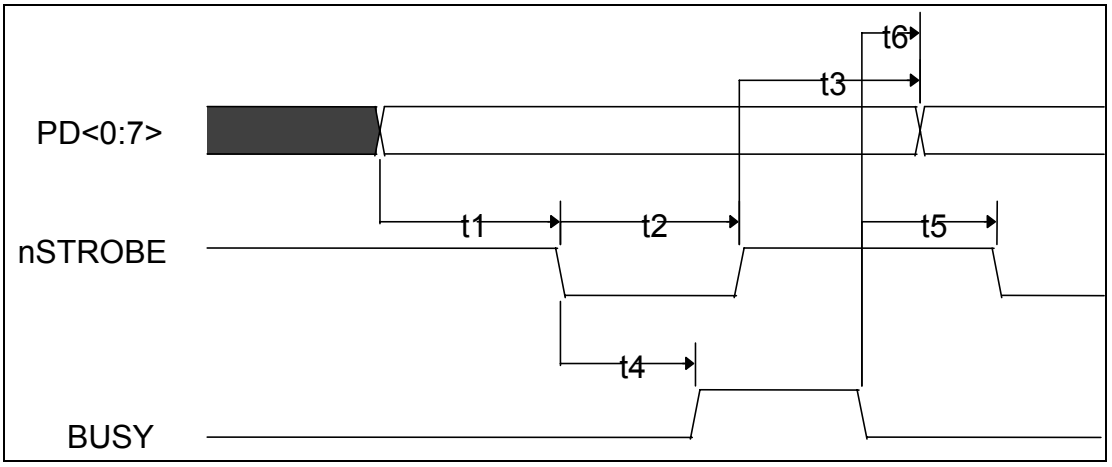


Figure 12.25 - Parallel Port FIFO Timing

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	PDATA Valid to nSTROBE Active	600			ns
t2	nSTROBE Active Pulse Width	600			ns
t3	PDATA Hold from nSTROBE Inactive (**Note 12.7**)	450			ns
t4	nSTROBE Active to BUSY Active			500	ns
t5	BUSY Inactive to nSTROBE Active	680			ns
t6	BUSY Inactive to PDATA Invalid (**Note 12.7**)	80			ns

Note 12.7 The data is held until BUSY goes inactive or for time t3, whichever is longer. This only applies if another data transfer is pending. If no other data transfer is pending, the data is held indefinitely.

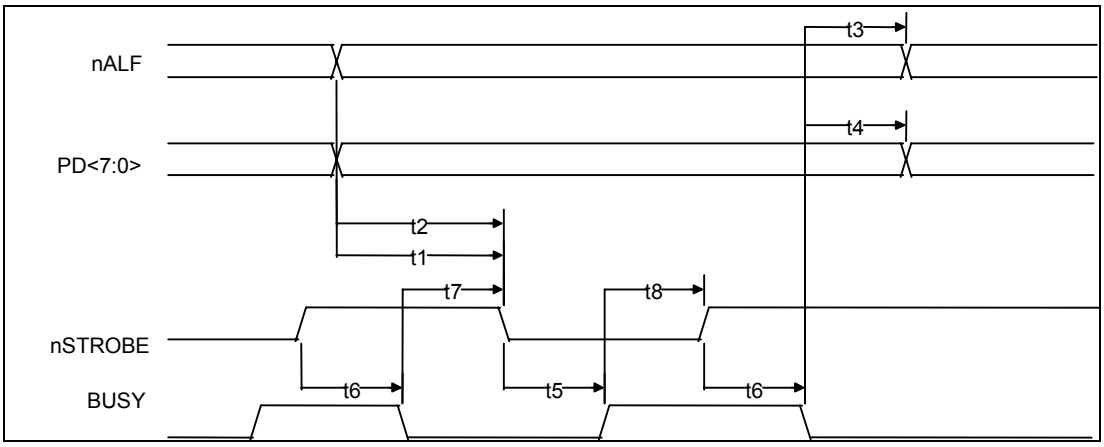


Figure 12.26 - ECP Parallel Port Forward Timing

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	nALF Valid to nSTROBE Asserted	0		60	ns
t2	PDATA Valid to nSTROBE Asserted	0		60	ns
t3	BUSY Deasserted to nALF Changed (**Note 12.8**, **Note 12.9**)	80		180	ns
t4	BUSY Deasserted to PDATA Changed (**Note 12.8**, **Note 12.9**)	80		180	ns
t5	nSTROBE Asserted to Busy Asserted	0			ns
t6	nSTROBE Deasserted to Busy Deasserted	0			ns
t7	BUSY Deasserted to nSTROBE Asserted (**Note 12.8**, **Note 12.9**)	80		200	ns
t8	BUSY Asserted to nSTROBE Deasserted (**Note 12.9**)	80		180	ns

Note 12.8 Maximum value only applies if there is data in the FIFO waiting to be written out.

Note 12.9 BUSY is not considered asserted or deasserted until it is stable for a minimum of 75 to 130 ns.

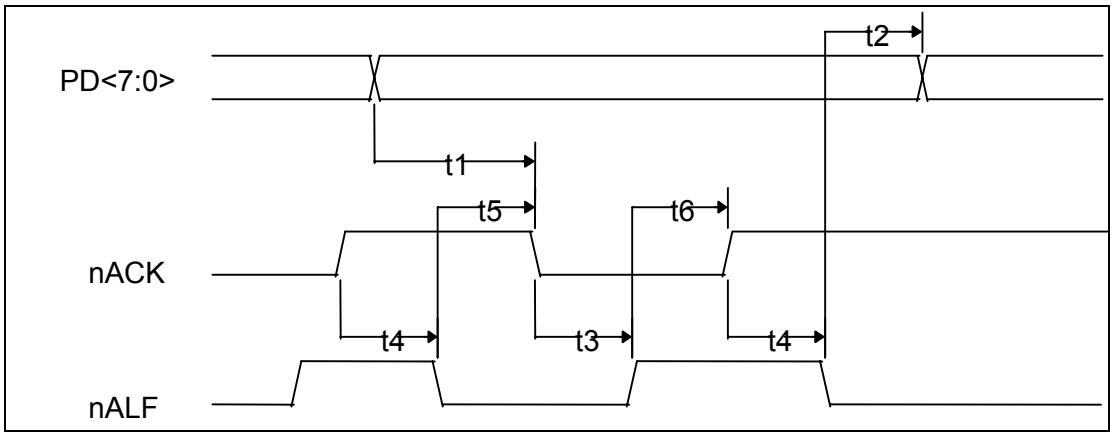


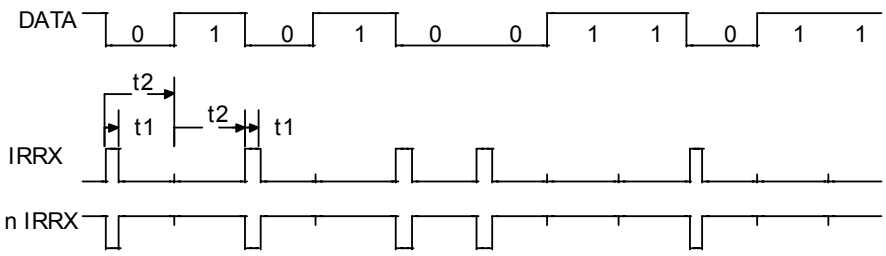
Figure 12.27 - ECP Parallel Port Reverse Timing

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	PDATA Valid to nACK Asserted	0			ns
t2	nALF Deasserted to PDATA Changed	0			ns
t3	nACK Asserted to nALF Deasserted (**Note 12.10**, **Note 12.11**)	80		200	ns
t4	nACK Deasserted to nALF Asserted (**Note 12.11**)	80		200	ns
t5	nALF Asserted to nACK Asserted	0			ns
t6	nALF Deasserted to nACK Deasserted	0			ns

Note 12.10 Maximum value only applies if there is room in the FIFO and terminal count has not been received. ECP can stall by keeping nALF low.

Note 12.11 nACK is not considered asserted or deasserted until it is stable for a minimum of 75 to 130 ns.

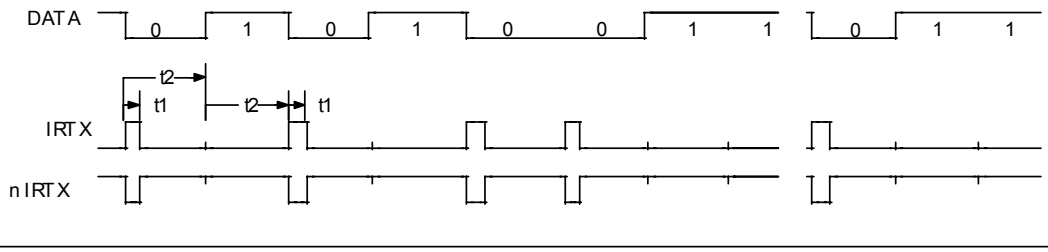
12.9 IR Timing



	Parameter	min	typ	max	units
t1	Pulse Width at 115kbaud	1.4	1.6	2.71	µs
t1	Pulse Width at 57.6kbaud	1.4	3.22	3.69	µs
t1	Pulse Width at 38.4kbaud	1.4	4.8	5.53	µs
t1	Pulse Width at 19.2kbaud	1.4	9.7	11.07	µs
t1	Pulse Width at 9.6kbaud	1.4	19.5	22.13	µs
t1	Pulse Width at 4.8kbaud	1.4	39	44.27	µs
t1	Pulse Width at 2.4kbaud	1.4	78	88.55	µs
t2	Bit Time at 115kbaud		8.68		µs
t2	Bit Time at 57.6kbaud		17.4		µs
t2	Bit Time at 38.4kbaud		26		µs
t2	Bit Time at 19.2kbaud		52		µs
t2	Bit Time at 9.6kbaud		104		µs
t2	Bit Time at 4.8kbaud		208		µs
t2	Bit Time at 2.4kbaud		416		µs

Notes:
1. Receive Pulse Detection Criteria: A received pulse is considered detected if the received pulse is a minimum of 1.41µs.
2. IRRX: L5, CRF1 Bit 0 = 1
   nIRRX: L5, CRF1 Bit 0 = 0 (default)

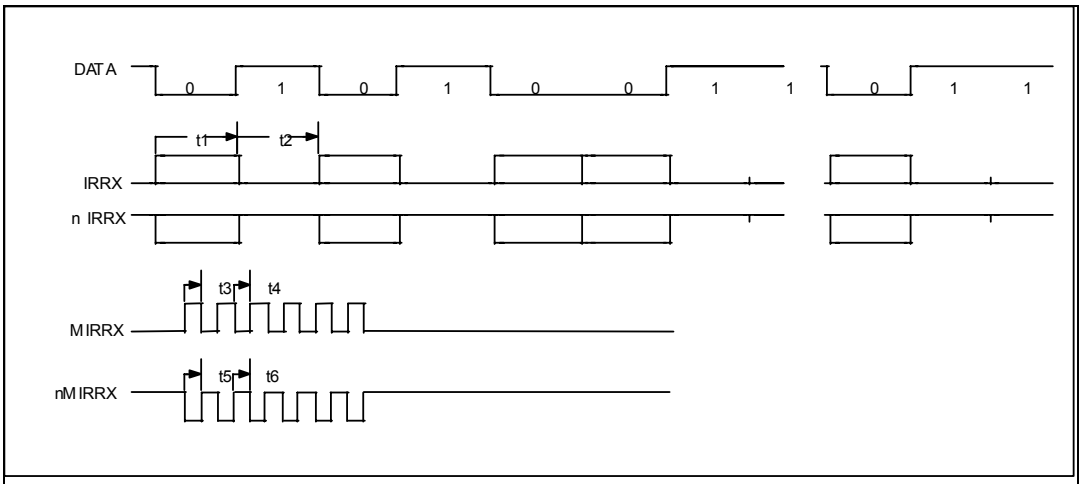
Figure 12.28 - IrDA Receive Timing



	Parameter	min	typ	max	units
t1	Pulse Width at 115kbaud	1.41	1.6	2.71	µs
t1	Pulse Width at 57.6kbaud	1.41	3.22	3.69	µs
t1	Pulse Width at 38.4kbaud	1.41	4.8	5.53	µs
t1	Pulse Width at 19.2kbaud	1.41	9.7	11.07	µs
t1	Pulse Width at 9.6kbaud	1.41	19.5	22.13	µs
t1	Pulse Width at 4.8kbaud	1.41	39	44.27	µs
t1	Pulse Width at 2.4kbaud	1.41	78	88.55	µs
t2	Bit Time at 115kbaud		8.68		µs
t2	Bit Time at 57.6kbaud		17.4		µs
t2	Bit Time at 38.4kbaud		26		µs
t2	Bit Time at 19.2kbaud		52		µs
t2	Bit Time at 9.6kbaud		104		µs
t2	Bit Time at 4.8kbaud		208		µs
t2	Bit Time at 2.4kbaud		416		µs

Notes:
1. IrDA @ 115k is HPSIR compatible. IrDA @ 2400 will allow compatibility with HP95LX and 48SX.
2. IRTX: L5, CRF1 Bit 1 = 1 (default)
   nIRTX: L5, CRF1 Bit 1 = 0

Figure 12.29 - IrDA Transmit Timing

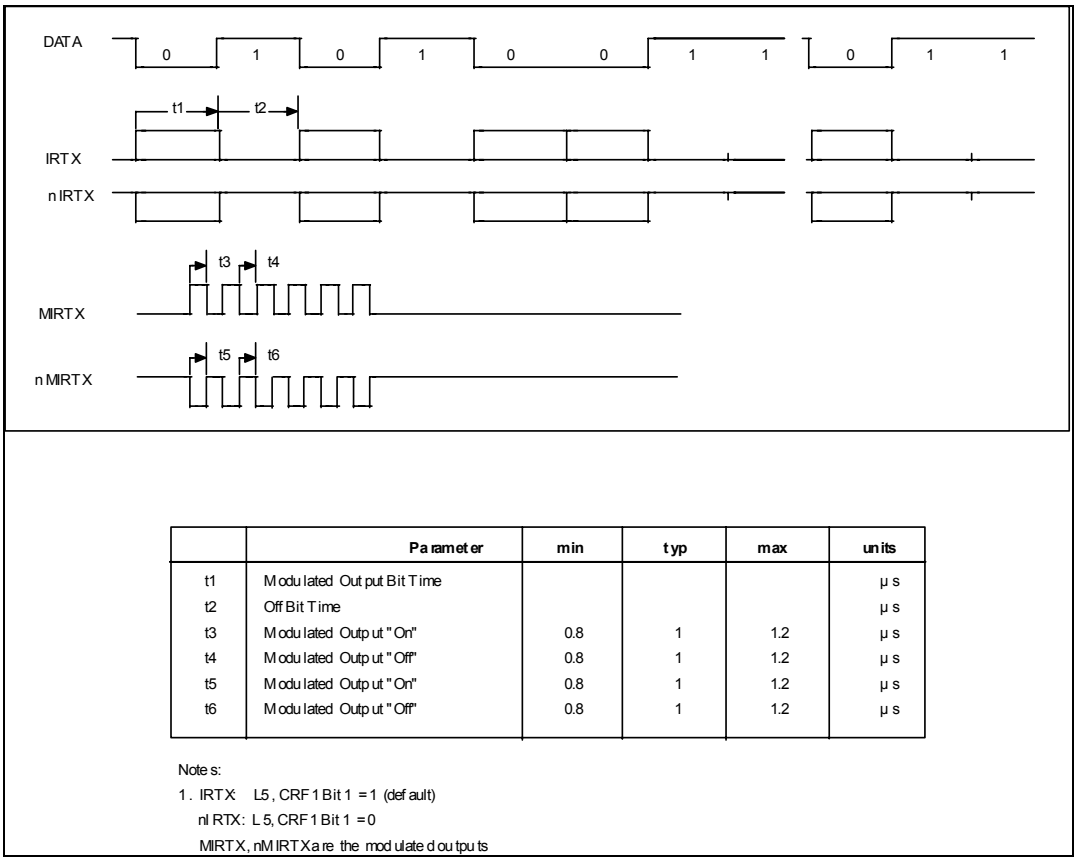


	Parameter	min	typ	max	units
t1	Modulated Output Bit Time				µs
t2	Off Bit Time				µs
t3	Modulated Output "On"	0.8	1	1.2	µs
t4	Modulated Output "Off"	0.8	1	1.2	µs
t5	Modulated Output "On"	0.8	1	1.2	µs
t6	Modulated Output "Off"	0.8	1	1.2	µs

Notes:

1. IRRX: L5, CRF1 Bit 0 = 1
   nIRRX: L5, CRF1 Bit 0 = 0 (default)
   MIRRX, nMIRRX are the modulated outputs

Figure 12.30 - Amplitude Shift Keyed IR Receive Timing



	Parameter	min	typ	max	units
t1	Modulated Output Bit Time				µs
t2	Off Bit Time				µs
t3	Modulated Output "On"	0.8	1	1.2	µs
t4	Modulated Output "Off"	0.8	1	1.2	µs
t5	Modulated Output "On"	0.8	1	1.2	µs
t6	Modulated Output "Off"	0.8	1	1.2	µs

Notes:
1. IRTX: L5, CRF1 Bit 1 = 1 (default)
nIRTX: L5, CRF1 Bit 1 = 0
MIRTX, nMIRTX are the modulated outputs

Figure 12.31 - Amplitude Shift Keyed IR Transmit Timing

12.10 Serial IRQ Timing

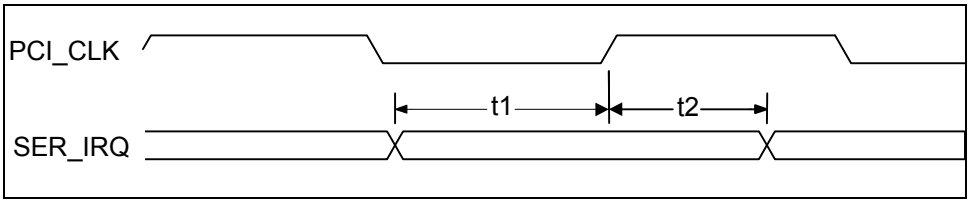


Figure 12.32 - Setup and Hold Time

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	SER_IRQ Setup Time to PCI_CLK Rising	7			nsec
t2	SER_IRQ Hold Time to PCI_CLK Rising	0			nsec

12.11 UART Timing

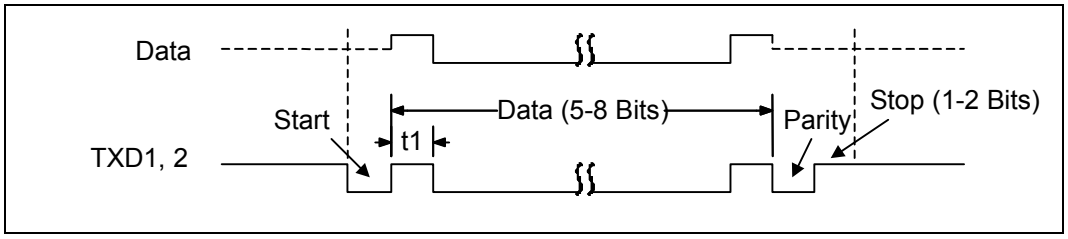


Figure 12.33 - Serial Port Data

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Serial Port Data Bit Time		t_{BR} (**Note 12.12**)		nsec

Note 12.12 t_{BR} is 1/Baud Rate. The Baud Rate is programmed through the divisor latch registers. Baud Rates have percentage errors indicated in the “Baud Rate” table in the “Serial Port” section.

Chapter 13 XNOR-Chain Test Mode

The SIO10N268 provides board test capability through the implementation of XNOR chain. See following sub-sections.

XNOR-Chain test structure allows users to confirm that all pins are in contact with the motherboard during assembly and test operations. See Figure 13.1 below. When the chip is in the XNOR chain test mode, setting the state of any of the input pins to the opposite of its current state will cause the output of the chain to toggle.

The XNOR-Chain test structure must be activated to perform these tests. When the XNOR-Chain is activated, the SIO10N268 pin functions are disconnected from the device pins, which all become input pins except for one output pin at the end of XNOR-Chain.

The tests that are performed when the XNOR-Chain test structure is activated require the board-level test hardware to control the device pins and observe the results at the XNOR-Chain output pin.

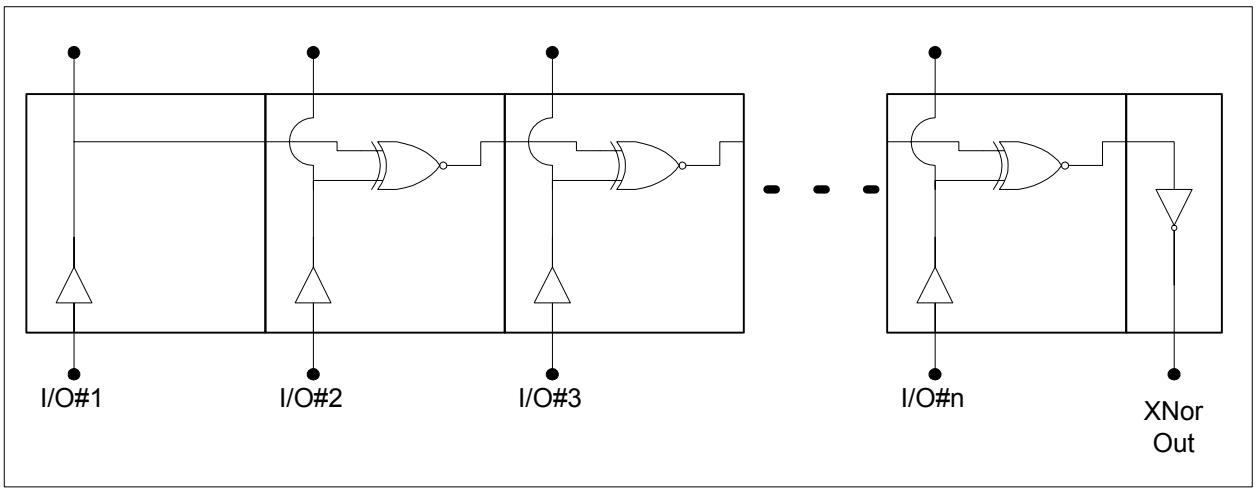


Figure 13.1 – XNOR-Chain Test Structure

13.1 Entering and Exiting Test Mode

To place a device into Test Mode, procedures should be followed according to the state of the LPC_ISA pin. That means if the LPC_ISA pin is left unconnected or is grounded, the device should be put into test mode using the procedures for LPC Mode. If the LPC_ISA pin is tied to VCC, the device should be put into test mode using the procedures for ISA Mode.

XNOR-Chain test mode can be entered as follows:

- Devices configured for LPC Mode (default – LPC_ISA pin is unconnected or tied to ground):
  - On the rising (deasserting) edge of PCI_RESET#, drive LFRAME# low and drive LAD[0] low.
- Devices configured for ISA Mode (LPC_ISA pin is tied to VCC):
  - On the falling (deasserting) edge of RESET_DRV, drive nIORD low and drive nIOWR low.

Exit XNOR-Chain test mode as follows:

- Devices configured for LPC Mode:
  - On the rising (deasserting) edge of PCI_RESET#, drive either LFRAME# or LAD[0] high.
- Devices configured for ISA Mode:
  - On the falling (deasserting) edge of RESET_DRV, drive either nIORD or nIOWR high

The PCI_RESET#, nRESET_DRV, and LPC_ISA pins are not included in the XNOR-Chain. The XNOR-Chain output pin# is 18, nIO_PME. See the following subsections for more details.

13.2 Pin List of XNOR Chain

Pins 1 to 128 on the chip are inputs to the first XNOR chain, with the exception of the following:

1) VCC (pins 25, 49, 70, 102, and 126) and VTR (pin 19).
2) VSS (pins 7, 27, 52, 74, and 109).
3) PCI_RESET# (pin 29), RESET_DRV (pin 59)
4) LPC_ISA (pin 54)
5) nIO_PME (pin 18) This is the chain output.

To put the chip in the first XNOR chain test mode:

LPC_Mode:

- Tie LAD0 (pin 21) and LFRAME# (pin 26) low. Then toggle PCI_RESET# (pin 29) from a low to a high state. Once the chip is put into XNOR chain test mode, LAD0 (pin 21) and LFRAME# (pin 26) become part of the chain.

ISA_Mode:

- Tie nIORD (pin 100) and nIOWR (pin 101) low. Then toggle RESET_DRV (pin 59) from a high to a low state. Once the chip is put into XNOR chain test mode, nIORD (pin 100) and nIOWR (pin 101) become part of the chain.

To exit the first XNOR chain test mode:

- Devices configured for LPC Mode (default – LPC_ISA pin is unconnected or tied to ground):
  - Tie LAD0 (pin 21) or LFRAME# (pin 26) high. Then toggle PCI_RESET# (pin 29) from a low to a high state.
- Devices configured for ISA Mode (LPC_ISA pin is tied to VCC):
  - Tie nIORD (pin 100) or nIOWR (pin 101) high. Then toggle RESET_DRV (pin 59) from a high to a low state.

NOTE: A VCC POR will also cause the XNOR chain test mode to be exited, regardless of the Mode. To verify the test mode has been exited, observe the output at nIO_PME (pin 18). Toggling any of the input pins in the chain should not cause its state to change.

13.3 Setup of XNOR Chain

WARNING: Ensure power supply is off during setup.

1) Connect VSS (pins 7, 27, 52, 74, and 109) to ground.
2) Connect VCC (pins 25, 49, 70, 102, and 126) and VTR (pin 19) to VCC (3.3V).

3) Connect test equipment to monitor output on nIO_PME (pin 18).
4) The LPC_ISA pin should be left unconnected or tied directly to ground if the device is implemented in LPC Mode. The LPC_ISA pin should be connected directly to VCC for devices that are implemented in ISA Mode.
5) If configured for LPC Mode, tie nLRESET and RESET_DRV/XA16 to ground. If configured for ISA Mode, tie RESET_DRV to VCC and tie nLRESET to ground.
6) All other pins should be tied to ground.

13.4 Testing Procedure

1) Turn power on.
2) Enter test mode as defined in section 13.1 Entering and Exiting Test Mode. The chip is now in XNOR chain test mode. At this point, all inputs to the first XNOR chain are low. The output, on nIO_PME (pin 18), should be high. Refer to INITIAL CONFIG on TRUTH TABLE 1.
3) Bring pin 128 high. The output on nIO_PME (pin 18) should toggle (i.e., nIO_PME = low). Refer to STEP ONE on TRUTH TABLE 1.
4) In descending pin order, bring each input high. The output should switch states each time an input is toggled. Continue until all inputs are high. The output on nIO_PME should now be low. Refer to END CONFIG on TRUTH TABLE 1.
5) The current state of the chip is now represented by INITIAL CONFIG in TRUTH TABLE 2.
6) Each input should now be brought low, starting at pin one and continuing in ascending order. Continue until all inputs are low. The nIO_PME output should now be high. Refer to TRUTH TABLE 2.
7) To exit test mode follow the procedures outlined in section 13.1 Entering and Exiting Test Mode.

TRUTH TABLE 1 - Toggling Inputs in Descending Order

	PIN 128	PIN 127	PIN 125	PIN 124	PIN 123	PIN ...	PIN 1	OUTPUT PIN 18
INITIAL CONFIG	L	L	L	L	L	L	L	H
STEP 1	H	L	L	L	L	L	L	L
STEP 2	H	H	L	L	L	L	L	H
STEP 3	H	H	H	L	L	L	L	L
STEP 4	H	H	H	H	L	L	L	H
STEP 5	H	H	H	H	H	L	L	L
…	…	…	…	…	…	…	…	…
STEP N-1	H	H	H	H	H	H	L	H
END CONFIG	H	H	H	H	H	H	H	L

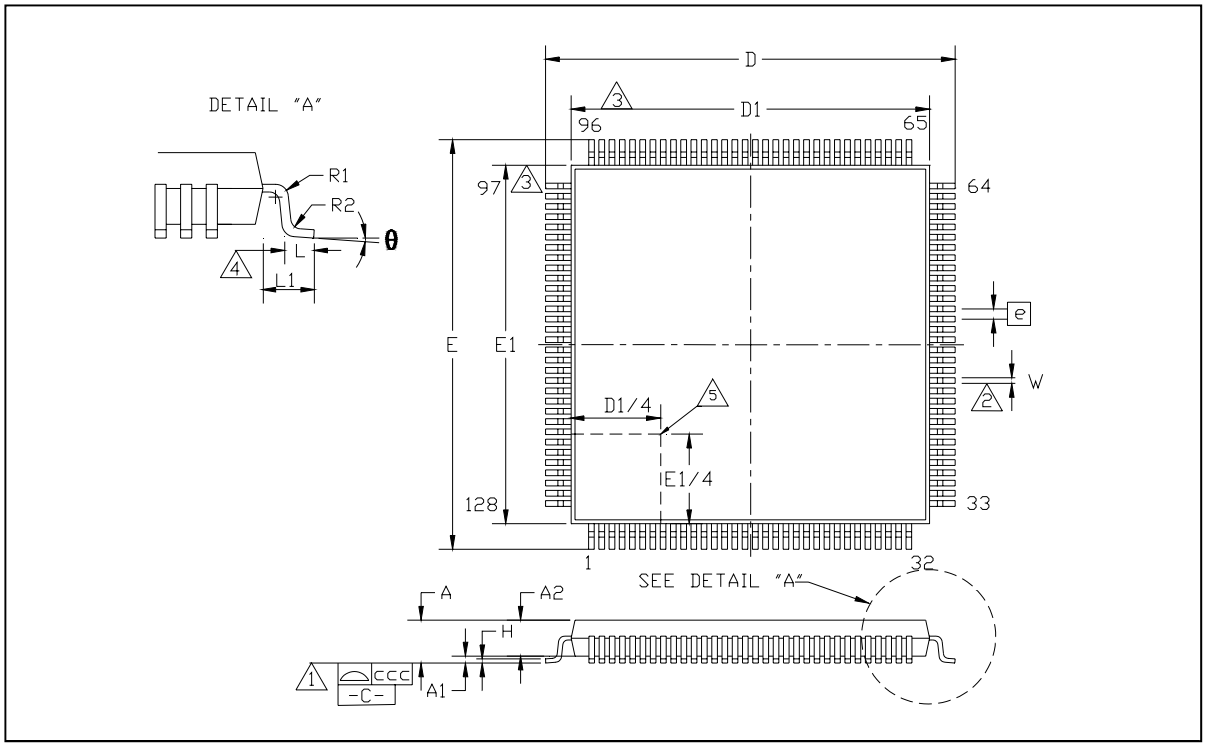
TRUTH TABLE 2 - Toggling Inputs in Ascending Order

	PIN 1	PIN 2	PIN 3	PIN 4	PIN 5	PIN ...	PIN 128	OUTPUT PIN 18
INITIAL CONFIG	H	H	H	H	H	H	H	L
STEP 1	L	H	H	H	H	H	H	H
STEP 2	L	L	H	H	H	H	H	L
STEP 3	L	L	L	H	H	H	H	H
STEP 4	L	L	L	L	H	H	H	L

	PIN 1	PIN 2	PIN 3	PIN 4	PIN 5	PIN ...	PIN 128	OUTPUT PIN 18
STEP 5	L	L	L	L	L	H	H	H
	…	…	…	…	…	…	…	…
STEP N-1	L	L	L	L	L	L	H	L
END CONFIG	L	L	L	L	L	L	L	H

Chapter 14 Package Outline

14.1 128 Pin TQFP Package Outline, 14x14x1.0 Body, 2 MM Footprint



	MIN	NOMINAL	MAX	REMARKS
A	~	~	1.20	Overall Package Height
A1	0.05	~	0.15	Standoff
A2	0.95	~	1.05	Body Thickness
D	15.80	~	16.20	X Span
D1	13.80	~	14.20	X body Size
E	15.80	~	16.20	Y Span
E1	13.80	~	14.20	Y body Size
H	0.09	~	0.20	Lead Frame Thickness
L	0.45	0.60	0.75	Lead Foot Length
L1	~	1.00	~	Lead Length
e		0.40 Basic		Lead Pitch
θ	0^o	~	7^o	Lead Foot Angle
W	0.13	0.18	0.23	Lead Width
R1	0.08	~	~	Lead Shoulder Radius
R2	0.08	~	0.20	Lead Foot Radius
ccc	~	~	0.08	Coplanarity

NOTES:

[1] Controlling Unit: millimeter.

[2] Tolerance on the true position of the leads is ± 0.035 mm maximum.

[3] Package body dimensions D1 and E1 do not include the mold protrusion. Maximum mold protrusion is 0.25 mm.

[4] Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane.

[5] Details of pin 1 identifier are optional but must be located within the zone indicated.

Chapter 15 References

1) SMSC Infrared Communications Controller (IrCC) Specification, dated 5/10/96
2) IEEE 1284 Extended Capabilities Port Protocol and ISA Standard, Rev. 1.14, July 14, 1993.
3) PCI Bus Power Management Interface Specification, Rev. 1.0, Draft, March 18, 1997.
4) Low Pin Count (LPC) Interface Specification, Revision 1.0, September 29, 1997, Intel Document.
5) Advanced Configuration and Power interface Specification, Revision 1.0